ELECTRICAL AND STRUCTURAL PROPERTIES OF High-k HfO$_2$ on Si$_{1-x}$ Ge$_x$ SUBSTRATES


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The changes in the electrical and physical properties of HfO$_2$ films grown using atomic layer deposition (ALD) on Si$_{1-x}$Ge$_x$ (x=0.1, 0.2, 0.3) substrates after post-annealing have been studied. The migration of Ge plays a key role in reducing the capacitance equivalent thickness (CET) whilst keeping the leakage current density constant after post-annealing. The Ge atoms which have already diffused into the HfO$_2$ upper layer during deposition are drawn back to interfacial layer. Although the thickness of interfacial layer increases, the thickness shrinkage of HfO$_2$ upper layer and increased permittivity of both layers achieves a reduction of the capacitance equivalent thickness.

INTRODUCTION

High-k HfO$_2$ gate dielectric films have been investigated intensively for several years and showed promising electrical properties [1,2]. However, the degradation of the carrier mobility in metal oxide field effect transistors (MOSFETs) is still a critical problem of the high-k/Si system. This effect can be compensated by the adoption of Si$_{1-x}$Ge$_x$ (x=0.1, 0.2, 0.3) as substrate material which has an enhanced carrier mobility compared to silicon [3]. However, complex interfacial reactions between the high-k material and the Si$_{1-x}$Ge$_x$ substrate adversely interfere with the electrical performance of the films. Several studies on the oxidation of Si$_{1-x}$Ge$_x$ showed that non-stoichiometric GeO$_x$ formation and metallic Ge segregation in the IL play a main role in the degradation of the electrical properties. The initial oxidation of the substrate is inevitable during ALD of the HfO$_2$ films. Therefore, the formation of a defective IL was expected. In this paper, the changes in the electrical and structural properties of the ALD HfO$_2$ films caused by the behavior of Ge were studied. Especially, the behavior of Ge components in the IL and its effects on the electrical properties before and after post deposition annealing (PDA) were investigated in detail.

EXPERIMENTAL PROCEDURE

HfO$_2$ with a nominal thickness of 3–7nm was grown on (100) Si and Si$_{1-x}$Ge$_x$ substrates in a 4” atomic layer deposition reactor (Ever-tek. Co, Plus-100) using Hf[N(CH$_3$)$_2$]$_4$ as Hf source. As oxidant O$_3$ with a concentration of 400g/m$^3$ was used. Details of the deposition processes were reported earlier [4]. The Si$_{1-x}$Ge$_x$ epitaxial layers of 30nm with various Ge concentrations (10, 20, and 30%) were grown on a (100) p-type Si wafer by low-pressure chemical vapor deposition (Jusung Engineering Co., Ltd.).
resolution X-ray diffractometry revealed that the Si$_{1-X}$Ge$_X$ epitaxial layer was strained coincidently with the lattice of the silicon substrate. PDA was performed using RTA at 800°C for 1 min under N$_2$ atmosphere after the film deposition. Electron beam evaporated platinum was deposited as top electrode for fabricating metal-insulator-semiconductor (MIS) capacitors. Forming gas annealing was performed at 400°C for 30 min under 95% N$_2$/5% H$_2$ atmosphere after the Pt top electrode deposition. Capacitance - voltage (C-V), leakage current-voltage (J-V), flat band voltage shift, and hysteresis characteristics were studied by using an HP 4194 impedance analyzer and an HP 4140B picoammeter/DC voltage source. The capacitance equivalent thickness (CET) was calculated from the accumulation capacitance. The depth profiles of the chemical composition of the film stacks were investigated by secondary ion mass spectroscopy (SIMS). Structural investigation was performed by using a high-resolution transmission electron microscope (HRTEM) equipped with a field emission gun. The chemical bonding status of the interface was studied by X-ray photoelectron spectroscopy (XPS).

RESULTS AND DISCUSSION

Figure 1 shows that an increased content of Ge of the substrate decreases CET after PDA, while it increases CET of the as-deposited state. Considering the larger oxidation rate of Si$_{1-X}$Ge$_X$ [4], a thicker low-k IL is formed and CET increases as the Ge concentration increases. This supports the trends which can be seen in the as-deposited samples [5]. However, the results from the PDA samples cannot be explained by the known oxidation mechanism of Si$_{1-X}$Ge$_X$. Therefore, it is expected that the electrical and structural changes of films on Si$_{1-X}$Ge$_X$ caused by PDA are different from those caused by the oxide formation in the well-known high-temperature thermal oxidation. In order to confirm the difference in the Ge oxidation behavior some of the Si$_{1-x}$Ge$_x$ layers were thermally oxidized using the O$_3$ at the same temperature as that of the HfO$_2$ ALD.

Figure 2 (a) shows the change in CET of thermal oxides using O$_3$ on Si$_{1-X}$Ge$_X$ as a function of the Ge concentration in the substrate. Oxidation was performed at 300°C for 1 h in O$_3$, and the samples were annealed using RTA under the N$_2$ atmosphere. It is interesting to note that the CET decreases as a function of the Ge concentration although the larger amount of Ge enhances the oxidation rate. This higher oxidation rate results in a thicker oxide. To understand this XPS of the samples were performed and the oxidation behaviors of Si and Ge were investigated under this oxidation condition.
Comparing the relative XPS peak intensity of the oxides and the substrate (Fig. 2 (b)), the oxide peak intensity ratios of both the Si and Ge increase with increasing Ge content, which means a faster oxidation rate of the Si$_{1-X}$Ge$_X$ in proportion to the Ge content. Therefore, considering these two graphs, it can be understood that the small CET originates from the higher permittivity of Si-Ge-O compared to SiO$_2$. A similar phenomenon appears in the case of HfO$_2$ on Si$_{1-X}$Ge$_X$ as mentioned previously. However, a higher permittivity of SiGeO is not enough to explain the strong CET reduction in HfO$_2$ on Si$_{1-X}$Ge$_X$.

Figure 3 shows the variation in the hysteresis in C-V curves of the thermal oxide formed by O$_3$ at 300°C and HfO$_2$ on the oxide in the as-deposited state. While the hysteresis is almost zero in the case of thermal oxides, it increases largely in the case of HfO$_2$ deposition after oxidation in proportion to the Ge content in the substrate. It should be noted that the HfO$_2$ films were grown on the intentionally grown thermal oxides in this case. The hysteresis increases drastically due to an interfacial reaction between HfO$_2$ and the thermal oxide during HfO$_2$ deposition. Considering the increase of hysteresis with the increasing Ge content and the standard heat of the formation of SiO$_2$, GeO$_2$, and HfO$_2$ (-911 J/mol, -580 J/mol, -1118 J/mol), reduction of GeO$_x$ to Ge is expected to occur during HfO$_2$ deposition. The Ge in the film may work as the trap site which results in the large hysteresis.

After taking everything into consideration, the model shown in Figure 4 is proposed for the Ge behavior. Ge atoms, which have been reduced and have easily diffused into the upper layer (UL) in the as-deposited state, are drawn back into IL after PDA. Permittivity enhancement of all the layers and a thinning of the UL compete with an increment of the IL, which determines the total CET. The changes in the component profiles and the thickness of each layer are confirmed for this model as shown in Figs. 5 and 6.
Figure 5 shows that the UL thickness decreases whilst the IL thickness increases after PDA. This is caused by the Ge migration from UL to IL during PDA. This trend is enhanced as the Ge content increases because the amount of migrating Ge increases.

Figure 6 shows the changes in Ge and HfGeO in SIMS depth profiles. The Ge content decreases in U.L. and increases in IL. after PDA. These graphs also support the suggested model.

Figure 7 shows (a) Ge 3d and (b), (c) Si 2p core level XPS spectra of HfO$_2$ on Si$_{1-x}$Ge$_x$ before and after the PDA. In the Ge 3d spectrum, the peak locating at 28.1 eV corresponds to the substrate. The peak near the binding energy of 31 – 33 eV corresponds to the oxidized Ge. It can be understood that in the as-deposited sample the oxidized Ge peak locates in lower binding energy position (~31.8 eV) suggesting that most of Ge exists in UL as Hf-Ge-O. That of the annealed sample locates in the higher binding energy position (~32.3 eV) suggesting that the Ge exists as GeO$_2$ or Si-Ge-O in IL. This
is also confirmed by the Si 2p spectrum shown in Fig. 7 (b) and (c); the Si-Ge-O peak increases after PDA (peak near the binding energy of ~ 102 eV).

Figure 8 shows a plot of the leakage current density versus CET of HfO$_2$ on Si$_{1-x}$Ge$_x$ before and after PDA. The arrows show the variation in the $J_g$ vs CET performance with the increase in Ge content. The leakage current density levels of the various samples become similar after PDA. It is very important that a reduction of CET can be achieved without increasing the gate leakage current density by an adoption of Si$_{1-x}$Ge$_x$ which has a higher carrier mobility compared to Si.

CONCLUSIONS

The changes in the electrical and physical properties of HfO$_2$ films on a Si$_{1-x}$Ge$_x$ after post-annealing have been studied. Ge plays an important role in reducing CET after post-annealing. This originates from an increase in the permittivity of the film and a decrease in the physical thickness of upper layer due to a drive-out of Ge after PDA which has already diffused into upper layer during deposition. Although CET decreases in proportion to the Ge content after PDA, the leakage current density level is maintained.

REFERENCES