A Fully Monolithic Wireless Display System

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We present a fully monolithic wireless interface for mobile displays, fabricated with CG-Silicon thin film transistors. The new interface uses a proprietary technique to wirelessly transfer both the image data and power for the LCD and backlight. Experimental results are presented from a 2.2” QVGA prototype demonstrating 100% wireless operation.

1. Introduction

The convergence of information technology, audio-visual technology and communication technology is driving mobile devices to offer ever increasing multi-media capabilities. At the heart of these devices, the high performance active matrix LCD (AMLCD) has become a window for communication and interactivity in the ubiquitous society. The advent of advanced low-temperature thin film transistor (TFT) processes, such as Sharp’s Continuous Grain (CG) Silicon technology, has made it possible to fabricate ‘System LCDs’, which feature data drivers, ambient sensors, touch sensors with scanning capability and other functional elements integrated directly onto the display substrate (1), (2), (3), (4). This paper addresses the latest developments in this field, namely the provision of monolithic wireless connectivity.

We will introduce the background to the type of wireless connectivity adopted in this work and provide a brief description of the system architecture. We will then describe the implementation of the key circuit components before finally presenting the experimental results and conclusions.

2. Wireless Communications

At the physical level, radio frequency communication systems can be broadly classified into two main categories. These are the conventional far-field systems which convey information in the form of propagating electromagnetic plane waves, and near-field systems that rely on vicinity inductive coupling using stationary magnetic fields. The main distinction between the two categories is determined by the relationship between the wavelength of the carrier, \(\lambda\), and the operating distance from the transmitter antenna. Near-field systems operate within a radius \(r = \lambda/2\pi\), around the transmitter. On the other hand, most mobile communication standards operate in the far field regime, beyond this radius, often with carrier frequencies in the 2.4 GHz ISM band. Whilst developments in GHz-capable CG-Silicon TFTs, with fine design rules and thin gate oxides, have been reported (5), this paper focuses on a novel wireless communication link which operates in the near-field regime. This category of wireless connectivity has found widespread application in Radio Frequency Identification (RFID) tags and more recently in Near-Field Communications (NFC) systems, operating in the internationally available 13.56 MHz ISM band.
MHz ISM band. Key advantages of such near-field links include the intuitive appeal of initiating communication between mobile devices simply by bringing them in close proximity to each other and that the short range link has obvious security benefits. In the next section we report on a highly compact full monolithic ‘display card’ demonstrator which is capable of wirelessly receiving image data and power when brought in close proximity to a transmitter.

3. System Architecture

A block diagram of the wireless display demonstrator is shown in Figure 1.

![Block Diagram of the Wireless Display Demonstrator](image)

**Figure 1. Overview of the wireless display demonstrator**

The system consists of a receiver system and a display module. This work focuses primarily on the design of the receiver system. The receiver is fabricated in a 1.5µm CG-Silicon process and comprises: an analogue front end, a digital processing section and an output driver. The display module is a 2.2” driver-monolithic QVGA display with framebuffer and display controller mounted on the flexible printed connector (FPC).

In the analogue front end, the transmitted signal is picked-up by a monolithic antenna. The output from the antenna is fed into a power rectifier and a data rectifier. The power rectifier supplies power to the receiver and the entire display module via voltage regulators, whilst the data-rectifier recovers the data signals. The analogue section also consists of a hardware reset system which clears all registers when the wireless display is placed in proximity to the transmitter. The digital section comprises a Manchester decoder, synchronization circuits, serial to parallel conversion and an output driver. The circuits are implemented on a glass substrate mounted behind the display module as shown in Figure 2.
In the next section we discuss the implementation of the key circuit components of the system.

### 4. Circuit Implementation

a) **Antenna System**

In the previous publication (6), we proposed an antenna that relied on a novel combination of series-parallel tuned circuit to obtain sufficient bandwidth and deliver the required power to the display module. Figure 3 shows the transfer function of this antenna system showing broadband response and good quality factor (Q) for efficient power transfer.

This antenna is highly effective in the 13.56 MHz ISM band, where the EMI emissions limits are less restrictive. In more restrictive frequency bands, capping the EMI emissions is a great challenge for this antenna. Sharp Laboratories of Europe Limited is developing a proprietary technique that reduces the emissions to almost zero whilst achieving both high bandwidth and very efficient power transfer.
b) **Rectifiers**

Both the power and data rectifiers are implemented as TFT-based full-wave bridge rectifiers comprising two p-type TFTs (M1, M2), two n-type TFTs (M3, M4) shown in Figure 5. \( C_L \) is a smoothing capacitor.

![TFT full wave bridge rectifier](image)

Figure 5. TFT full wave bridge rectifier

The sizing of the TFTs in the bridge is a compromise between its current handling capability and the effective capacitance presented to the antenna. The size of the capacitance affects the kind of matching network needed between the antenna and the TFT-bridge rectifier.

c) **Voltage Regulators**

Since the link supplies the power for the display module, it is essential to use some form of voltage regulation to ensure the stability of the operating voltage as a function of operating distance. This is achieved with the monolithic voltage regulator design shown in Figure 6.

![Voltage regulator to supply the 1.8 V to the display module](image)

Figure 6. Voltage regulator to supply the 1.8 V to the display module
d) **Demodulator**

The demodulator circuit is responsible for recovering the data from the amplitude modulated signal generated at the output of the data rectifier. The circuit diagram for the demodulator is shown in Figure 7.

The signal recovered from the data rectifier has a dc level nearly that of the power supply. The level shifter, implemented using a source follower, lowers this value to the mid-supply voltage. To reduce the occupied space, the source resistor of the level shifter is implemented as two diode-connected loads in parallel. The signal is then amplified and low-pass filtered. The output of the demodulator is a comparator that compares the filtered and unfiltered signals to obtain the demodulated digital signal. Figure 8 shows the simulation outputs for different parts of the demodulator.

![Demodulator Circuit Diagram](image)

**Figure 7. ASK Demodulator**

![Simulation Outputs](image)

**Figure 8. Simulation outputs for different parts of the demodulator**
e) **Master Clock Generation**

The master clock is derived from the carrier using the carrier digitizing circuit shown in Figure 9. One of the challenges when designing circuits using thin-film transistor technology is obtaining stable biasing voltages. In this work, considerable effort was made to make sure that the majority of the circuits were implemented using self-biasing architectures. Figure 9 is an example of a robust self-biasing comparator capable of withstanding large variations in the process conditions.

![Diagram of Master Clock Generation](image)

**Figure 9. Master Clock Generation by a Digitizing Circuit**

Figure 10 shows the simulated input and output signals of the carrier digitizer.

![Simulated input and output signals](image)

**Figure 10. Simulated input and output signals of the carrier digitizer used to generate the master clock.**
f) Manchester Decoder

In order to preserve a timing of the signals, the transmitted data is encoded using a self-clocking code such as Manchester. In Manchester encoding, a ‘1’ represented by a Low-to-High transition, a ‘0’ represented by a High-to-Low transition. This is shown Figure 11.

![Manchester Encoding Process](image)

Figure 11. Manchester encoding process

The purpose of the Manchester decoder is to regenerate the data and clock from the demodulator output. Figure 12 shows the block diagram for our implementation of the Manchester decoder.

![Manchester Decoder Block Diagram](image)

Figure 12. Manchester Decoder Block Diagram

The 8x over-sampling clock is obtained from the master clock generated by the carrier digitiser. Figure 13 shows waveforms at various stages of the Manchester Decoder.
g) Serial to Parallel Converter

As shown in Figure 14, the serial-to-parallel converter consists of 4 blocks:

- 9-bit shift register;
- Parallel transfer register;
- Digital output buffer;
- Divide by 9 counter and signal generator.

The 9-bit shift register is serially loaded with one frame of data which is then sampled and latched by the parallel transfer register at the end of every frame. The divide by 9 counter is responsible for generating a pulse at the end of every frame to control this register transfer operation. The counter also generates the write-enable signal (WRX) required by the display module.
h) Reset Sequence Detector (Synchronisation)

The reset sequence detector is required to correctly synchronise the receiver circuits to the transmitter in order to initiate communication. To achieve this, a unique data sequence is required. This reset sequence must not occur in normal operation and, furthermore, it must be detectable even though the receiver has not been synchronized. One such unique sequence for the display module used in our design is a sequence of 2 consecutive frames (i.e. 18 bits) of ‘1’s. This can be used to drive the system into and out of reset. In Figure 15, SDATA is the synchronisation sequence. The first 18 bits of 1’s drive the system into reset (RSTB). This is followed by sequence, unrecognizable by the sequence detector, whose duration determines the time the system is in reset. A further sequence of 18 bits of 1’s takes the system out of reset. At this point the frame is synchronised.

![Figure 15. Frame synchronisation process](image)

5. Experimental results

In order to demonstrate the potential of the wireless display and to test the capability of the receiver, an experimental display-card prototype was designed. The transmitter uses Amplitude Shift Keying (ASK) to modulate a 27MHz carrier, using the new proprietary antenna system. The data and control signals for the display are Manchester encoded prior to being transmitted at a data rate of 3.375 Mbps. The transmitter includes impedance monitoring circuits to detect the presence of a wireless display using the ‘load modulation’ principle. Once a display is within 1cm of the transmitter a reset sequence is initiated and data transmission begins. The data is demodulated in the receiver and continuously frame-buffered prior to display. Figure 16 shows the wireless display module receiving image data and power from the transmitter antenna.
6. Conclusions

We have demonstrated for the first time a monolithic wireless display interface using CG-Silicon technology. The interface is capable of transmitting image data and power to a QVGA LCD module over a distance of 1cm.

Future developments will include further developments on the antenna system and receiver to enable full monolithic integration with a display. The system will also be implemented using a variety of carrier frequencies and data rates according to continuous advances in process technology and application requirements.

We believe this result is a significant step towards the ‘System-On-Panel’ concept and will offer a variety of applications in highly portable personal displays.

References