Current challenges with copper interconnects

Paul R. Besser
Technology Research Group, Advanced Micro Devices, Inc.
One AMD Place, Mail Stop 36, Sunnyvale, California, 94088 USA

Abstract

In the integrated circuit industry, aluminum-based interconnects and oxide interlayer dielectrics have been replaced with copper interconnects in a dual inlaid architecture and with low-K dielectrics. Inlaid Cu lines offer higher conductivity, improved electromigration performance and a reduced cost of manufacturing. In this manuscript, the current challenges with integrating Cu in high-performance integrated circuits are detailed. As technologies scale, the many steps in the integrated process flow cannot be viewed as independent. The interactions between process steps (module interactions) that must be considered will be discussed. The development of a reliable and manufacturable technology requires a fundamental understanding of these interactions. A process-oriented finite element model (FEM) will be presented to capture the effect of individual process steps on the stress evolution during processing. Finally, the future trends for Cu interconnect will be suggested.

Introduction

In the microelectronics industry, leading-edge microprocessors contain more than 200 million transistors and can operate at speeds in excess of 4 GHz. The interconnect complexity has increased with the number of transistors, and 8-11 layers of high-density interconnects are commonly used to connect transistors into circuits and microprocessors. In order to increase the speed and to reduce manufacturing costs, the critical dimensions are consistently reduced with each technology node. As the dimensions of the interconnect lines shrink, aluminum-based interconnects and oxide interlayer dielectrics have been replaced with copper interconnects in a dual inlaid architecture with low-K (K=dielectric constant) dielectrics (1-3). Inlaid Cu lines offer higher conductivity, improved electromigration performance and a reduced cost of manufacturing; however, the inlaid fabrication method and the introduction of low-K dielectrics to improve performance present a host of integration and reliability challenges (1-4).

Figure I illustrates the evolution of the back-end of line (BEoL) interconnects from the 180nm technology node to the 90nm technology node. At the 180nm technology node, six layers of Cu interconnects were used, while at the 130 and 90nm nodes, nine layers of Cu interconnects were implemented. At the 65nm technology node, eleven layers of metal are expected. Copper/low K is part of the current 65nm technology generation which is being ramped into volume manufacturing. The next generation technology (45nm) is being developed and the next-next generation (32nm) is being researched. As the technology scales, product performance is increasingly dominated by interconnect
resistance and interlayer dielectric capacitance. As a result, advanced interconnect processes and materials must be seamlessly integrated and implemented to meet the product performance, reliability and cost requirements for current and future generations.

In this manuscript, the current challenges with integrating Cu in high-performance integrated circuits will be highlighted, and the trends for the future technologies will be suggested. A process-oriented finite element model (FEM) will be presented to capture the effect of individual process steps on the stress evolution in the BEoL. In this experimentally calibrated model, the complete stress history at any step of BEoL can be simulated as an inlaid Cu structure is fabricated, and the Cu line stress evolution during the process of multi-step processing can be determined. Finally, the interconnect trends for the future will be suggested.

![Copper interconnect scaling](image)

Figure I. The evolution of Cu interconnect technologies from the 180 to 90 nm technology nodes. The number of metal layers and the density increases with each node.

In order to highlight and review the current challenges with implementing Cu interconnects, it is useful to peruse a high resolution micrograph of a typical dual inlaid Cu structure (Figure II). The upper metal layer (M2) contacts the underlying metal layer (M1) through a via (C2), where the upper metal and via are lined with a barrier and filled with copper using a dual inlaid process sequence. In general, the fabrication of this interconnect is straightforward to visualize but not simple to implement into high-volume manufacturing. The process begins with the deposition of the dielectric stack. Metal lines and vias and lithographically patterned and etched to produce straight and smooth sidewalls with a slightly tapered line and via profile. In addition, any residuals at the via bottom must be removed by the etch processes. It is preferred to have the etch process gauge or recess into the underlying metal layer to “anchor” the via, reduce the electrical contact resistance, and enhance the stress-migration and electromigration reliability (5-6).
A barrier layer is typically deposited between the Cu and the dielectric to contain the Cu within the line. The barrier plays a pivotal role in the Cu interconnect integration. This barrier must be thin and continuous, have a low resistivity, promote good adhesion, and be a good barrier to Cu diffusion. The barrier metal must make good electrical contact to the underlying metal, and this requires removal of any etch residue at the via bottom as well as removal of any oxide on top of the underlying metal. Often, a pre-sputter clean is performed in-situ prior to or during barrier deposition by physical vapor deposition (PVD). Noting the high aspect ratio of the structure in Figure II, it can be appreciated that advanced and expensive sputter deposition methods are necessary to provide a thin and continuous barrier with minimal overhang and minimal field thickness.

Metallic barriers are the preferred interface to the Cu to provide the best electromigration (EM) performance; however, amorphous barriers are better diffusion barriers. Although their resistance might be high, conformal barriers deposited by chemical vapor, atomic layer or electrochemical deposition reduce the overall line resistance since they can be much thinner. Migration to a new material or a new deposition method is challenged by the manufacturing immaturity of the new deposition technology or material. All these considerations must be comprehended into the barrier metal choice. A multilayer barrier is often implemented that combines one material (TaN) which has good adhesion and is a good barrier to Cu diffusion together with a metallic barrier (Ta) for good EM.

The Cu metallization is deposited after the barrier metal. Typically, the thin Cu metallization layer is deposited on the barrier with PVD and the remainder of the via and line are filled with Cu using electrochemical deposition methods. To prevent barrier oxidation, the Cu is deposited in a different chamber of the same multi-chamber, ultra-high vacuum sputtering system as was used to deposit the barrier and perform the pre-clean. The Cu seed metal must be continuous and have good step coverage with little overhang. Often, the thickness of the seed layer is a balance between the minimum thickness needed to promote electrochemical deposition (ECD) and the maximum thickness where the overhang narrows the top opening. It follows that the deposited Cu thickness will have to reduce with narrower linewidths, or the sputtering technology has to continually improve. Of course the Cu must fill the line and via void-free for all lines and vias across each dice of each wafer, day in and day out, for hundreds of wafers a day and 8-11 layers of metal.
Once filled with Cu and annealed to increase the grain size, evolve impurities, and reduce the line resistance, the overburden or excess Cu and barrier are removed with chemical mechanical polishing to electrically isolate the Cu interconnect lines. In addition, the Cu lines must be capped with a dielectric that contains the Cu and adheres well to the Cu. Many manufacturers are considering improvements to the adhesion of the cap to the Cu or the insertion of a metal cap onto the Cu, prior to the dielectric deposition, in order to improve reliability of Cu interconnects with scaling (7-8), including the commercially available, selectively-deposited, metallic capping layer CoWP.

The Cu interconnect formation process faces many challenges as the dimensions of the interconnect lines are scaled with technology node. The many steps in the process flow cannot be viewed as independent knobs that can be optimized independently of other steps in an integrated process flow. Module interactions must be considered. For example, the dielectric (ILD) modulus of elasticity (E) and coefficient of thermal expansion (CTE) depend on ILD type and stack. The dielectric type determines both the etch and ash process, which determine the sidewall profile for metal fill, and the etchability of residuals at the via bottom. The barrier metal and Cu seed profile and thickness influence the plating process and choice of additives. The metal stack and dielectric each provide constraints on the CMP process. The CMP process determines the line resistance variation across the wafer and topography/planarity for subsequent metal layers. The aspect ratio, barrier sputter profile, and Cu sputter profile directly affect the plating process. The plating and anneal process affect the grain growth and mechanical stress of the Cu interconnect line. The dielectric material, barrier type, cap layer pre-process and type, CMP process, and anneal all affect reliability. Thus, the development of a reliable and manufacturable BEOL process requires a fundamental understanding of these and many other interactions.

In the endless need for improved speed and reduced cost, the integrated circuit industry will further scale the critical dimensions as it migrates from 90 to 65 to 45 to 32nm technology nodes. This technology shrinking presents interesting dilemmas to the integration, module development, process development and product design teams. Reducing dimensions laterally leads to narrower lines and smaller spaces between lines. Narrower lines typically have higher resistance. Of course the chip designers want to have a minimal line resistance increase from technology generation to generation. As shown in Figure III, the line resistance will increase with each technology node as the linewidth is decreased if the line aspect ratio is kept constant. In order to keep the designers happy with narrower lines, the aspect ratio will necessarily increase, creating major challenges to the barrier step coverage, the Cu step coverage and the Cu ECD fill processes. These modules must work together to guarantee void-free fill with increased aspect ratio. The needs of each stake holder in the integrated module must be balanced with the desires of the designers and the manufacturability and cost of the integrated module.

An additional dilemma created by technology scaling is how to handle the increase in capacitance between lines as a result of the reduced spacing between lines. A lower dielectric constant (K) material can be inserted between lines to reduce this capacitance, but with additional compromises. As illustrated in Figure IV, reducing the dielectric constant also reduces the modulus of elasticity of the insulating material (9). For low-K dielectrics commonly used in integrated circuits at the 90 and 65nm technology node (i.e. C-doped glasses), the modulus is significantly lower than that used in previous generations (i.e. FTEOS and oxide). This provides a significant challenge to the integration and also leads to reliability, stress, adhesion, and packaging issues.
Figure III. Metal line resistance is plotted as a function of technology node. The line resistance increases dramatically with scaling if a constant aspect ratio is assumed. If the aspect ratio is increased with each successive node, then the line resistance increase is less dramatic.

Figure IV. A plot of modulus of elasticity (E) as a function of dielectric constant (K) reveals that the modulus decreases with decreased dielectric constant. For the C-doped glasses commonly implemented at the 90 and 65nm technology node, the modulus is significantly lower (9).

Process-oriented modeling

The interaction of the individual process steps on the Cu interconnect module has been highlighted thus far, and it has been argued that process steps affect adjacent modules in ways that are not always intuitive. In order to better understand the influence of processing on the Cu interconnect, a process-oriented finite element model (FEM) was developed. This model captures the effect of individual process steps on the mechanical stress evolution in the BEoL. Details of the model, as well as assumptions and materials parameters have been published elsewhere (10-13). Briefly, the model assumes that linear
elasticity prevails for all materials without accounting for microstructure-dependent nonlinear behavior of Cu. A complete geometric model with final configuration is built that matches identically to the BEoL integration in dimension and materials properties. Deposition processes including CVD, electroplating, etch and CMP involve material addition or removal, as simulated by the elemental birth and death in the process-oriented modeling procedure. The well known intrinsic stress arising from deposition of dielectrics including SiO2, Si3N4 and carbon-doped oxide based low-K dielectrics is accounted for with the introduction of a virtual deposition temperature. Table I lists the properties of materials used in the modeling (10, 14-17).

<table>
<thead>
<tr>
<th>Material</th>
<th>Modulus (GPa)</th>
<th>CTE (ppm/C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cu</td>
<td>115</td>
<td>17.7</td>
</tr>
<tr>
<td>Oxide</td>
<td>71.4</td>
<td>0.51</td>
</tr>
<tr>
<td>Spin on Low-K</td>
<td>6</td>
<td>20</td>
</tr>
<tr>
<td>CVD Low-K</td>
<td>2</td>
<td>66</td>
</tr>
</tbody>
</table>

The stress evolution in the Cu line is vital to understanding the reliability risk associated with process and material changes. With this model, the complete stress history at any step of BEoL can be simulated as a dual inlaid Cu structure is fabricated, and the Cu line stress evolution during the process of multi-step processing for dual inlaid Cu/low-K structures can be monitored. The model has been calibrated with both wafer-curvature blanket film measurements and X-Ray diffraction determination of metal line stress (11-12). Figure V shows three steps in the process flow as the model builds a dual inlaid M1-V1-M2 structure with a top passivation layer. The structure includes dielectrics at the metal layer, capping layer and via layer that can be independently changed. The structure is built in steps with layers added and subtracted, following a typical process flow. The structure spans only half of the pitch size in the Z-direction (out-of-plane) to take advantage of symmetry. Each layer (M1, V1 and M2) is patterned, etched, filled with barrier and Cu, and polished, then the next layer is processed. Details of the M1 structure are included in the cross-section in Figure V.

The model has been used to simulate complete stress history at any step of BEoL as a dual inlaid Cu structure is fabricated. The Cu line stress evolution was simulated during the process of multi-step processing for dual inlaid Cu/TEOS and Cu/low-k structures. It was found that the in-plane stress of Cu lines is nearly independent of subsequent processes, while the out-of-plane stress increases considerably with the subsequent process steps. The model was further applied to understand whether the coefficient of thermal expansion or modulus of the dielectric affects the Cu stress more significantly (12). It was found that the stress magnitude and state (hydrostatic, deviatoric) depend on ILD properties. The stress along the line length (longitudinal) is substrate-dominated, while the transverse and normal stresses vary with both CTE and modulus of the dielectric. These trends are consistent with experimentally determined stress values.

In addition to computing volume-averaged stresses at a global level, it is desirable to investigate the local stress field around the region of interest. With the presence of a via, the stress field at the vicinity of via/line junction is expected to be highly localized. Figure VI shows contour plots of hydrostatic stress around the via bottom, as determined by the model. The line surface beneath the via barrier has a higher compressive stress than the surrounding region. This explains why atoms are driven toward this region by a stress gradient. Figure VI (right) shows a failure analysis picture from a wide Cu line (5.4um) of a single via chain M1V1M2 of Cu/low-K (10). The stress-induced void is located at the lower corner of V1 within M1. Diffusion is assumed to be along the Cu/cap interface driven by the high stress concentration and the stress gradient associated with.
that region. The model provides insight into understanding real problems in the IC industry.

Figure V. Three steps in the process flow as the model builds an inlaid M1-V1-M2 structure with a top passivation layer are shown. The structure is built by adding and subtracting layers, following a typical process flow. The detailed M1 model (right) shows the barrier and dielectric layers ((11-12)).

Figure VI. The FEA model of Cu line and via (left) showing area of highest stress is adjacent to the via. SEM image (right) indicates that stress-induced voiding occurs in a similar spot (10).
The future of Cu interconnects

Looking forward to 45 and 32nm technologies, the concept of module interactions and process development being dependent on adjacent modules becomes even more important. All aspects of the Cu interconnect BEoL feel the strain of the high aspect ratios and the need for lower Cu resistance. Scaling of Cu interconnect technologies beyond the 45nm technology node may require the introduction of alternative deposition equipment and processes in order to guarantee void-free fill. As mentioned earlier, the Cu seed layer is one area where significant improvement is needed. PVD processes lead to large overhang that can pinch off the top of the line/via and create challenges for Cu electrochemical deposition. Thinning the Cu seed to enhance ECD fill of the line will also thin the Cu at its thinnest point (halfway up the sidewall), making this area susceptible to voiding when the Cu plating chemistry attacks the exposed barrier. Reducing the aspect ratio or improving the Cu sputtering technology is essential to scale Cu seed technology further. Cu seed is an example of one area where technology improvements are needed. The barrier technology faces similar challenges, albeit for different end goals previously described in this manuscript.

There are numerous publications on the subject of linewidth extendibility in Cu interconnects (18-20). The increase in the resistance of Cu as the linewidth is reduced is due to electron scattering events in the Cu, which include impurities in the Cu, interfaces, defects, grain boundaries, etc. Eventually, when the Cu linewidth is of the same magnitude as the electron mean free path in Cu (39nm), the Cu itself will become the resistance limiter. The IC industry will likely reach these dimensions at the 22nm technology node. Thus it is reasonable to expect Cu interconnects to scale to this technology node, once the scattering mechanisms are understood and reduced.

As the linewidth of Cu is scaled, it will be important to understand, quantify and reduce the contributions to scattering that can lead to resistance increases. Even though grain orientation and grain size have been shown to be second order contributors to reliability improvement, (3) grain growth studies are necessary in order to increase the grain size median and distribution. Many studies (17, 21-27) have been undertaken to quantify microstructure in trenches and models have been developed to understand the grain growth. For narrow lines, the inlaid fabrication method clearly influences the grain growth. Larger grains will minimize the grain boundary contribution to resistance, but it is difficult to get Cu grains in an inlaid interconnect line to grow within the thermal budget dictated by the low-K dielectric. Some modeling work is underway to further understand this grain growth (27). Additional sources of scattering, such as line edge roughness, are dictated by the lithography and etch modules.

For the purpose of the 2006 Electrochemical Society symposium on “Electrochemical processes for ULSI and MEMs”, there are many areas were electrochemical processes may enable continued scaling of Cu interconnect technology. These include barrier deposition, Cu fill, Cu capping, and CMP. Improvements in the conventional PVD barrier are needed, otherwise migration to a conformal barrier (TaN or Ta) or a different material (Ru, alloy) will be necessitated and should be developed now. Conformal barrier processes and novel materials require time to insert into the manufacturing line so that the manufacturability, integratability and reliability can be proven. Alternative electrochemical processes to enhance Cu seed step coverage or to enable conformal Cu fill will likely be required, and are being developed. In addition, research on novel capping layers will be important to create thin, selectively-deposited metallic caps which can improve electromigration and stress-migration reliability. Each of these research topics has tremendous potential to improve Cu interconnect performance, but none of them can be researched as an independent process step. Interactions with other modules must be comprehended.
Conclusions

The current challenges with integrating Cu in high-performance integrated circuits were detailed in this manuscript. The Cu interconnect process faces many challenges as the dimensions of the interconnect lines are scaled with technology node. The many steps in the integrated process flow cannot be viewed as independent. The module interactions must be considered. The development of a reliable and manufacturable BEOL process requires a fundamental understanding of these and many other interactions. To help with this understanding, a process-oriented finite element model (FEM) was presented to capture the effect of individual process steps on the stress evolution in the BEOL. Finally, the Cu interconnect trends for the future were suggested. Cu interconnects will extend through the 32nm technology node, although some advances in processing technology and/or new processing technology will be needed to enable this extendibility.

Acknowledgments

The author would like to thank the symposium organizers for the invitation to be the Keynote Speaker for the Symposium. The author thanks Charlie Zhai of AMD for the modeling contribution to the work, Todd Ryan of AMD for the modulus vs. dielectric constant input, and the following people for technical advice: Connie Wang, Christy Woo, and Wen Yu. Thanks to Liliana Thompson of the Materials Characterization Lab at AMD for providing the TEM in Figure II. AMD, the AMD Arrow Logo, AMD Athlon, AMD Opteron and combinations thereof are trademarks of Advanced Micro Devices, Inc.

References