Physics and Technology of High-\(k\) Gate Dielectrics 4

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PREFACE

General Observations

This issue of ECS Transactions (ECST) contains the full manuscripts of the forty seven presentations scheduled for The Fourth International Symposium on High Dielectric Constant Gate Stacks, to be held in Cancun, Mexico on October 30 to November 03, 2006. This symposium is cosponsored by the Dielectric Science and Technology Division and the Electronics and Photonics Division of The Electrochemical Society, and will be held during its 210th Meeting.

The first Symposium in this series was held in Salt Lake City, October 20-24, 2002, in which thirty four plenary, invited, and contributed papers were presented. The second Symposium in this series was held in Orlando, Florida, on October 12-17, 2003, in which fifty six invited and contributed papers were presented. The third Symposium in this series was held in Los Angeles, California, on October 17-20, 2005, in which eighty nine invited and contributed papers were presented.

This issue is divided into ten chapters, reflecting the sessions and the organization of the symposium. We will have a joint session with the symposium E3 (“Atomic Layer Deposition Applications 2”). Two of the manuscripts of the joint session, belonging to our symposium, are included in chapter 5.

At the third symposium of the series on high dielectric constant gate stacks, we introduced a new feature - the best paper award, which was won by Maureen MacKenzie of the University of Glasgow, UK, on the basis of her presentation and her manuscript entitled, “Advanced Nano-Analysis of High-K Dielectric Stacks”. The award was made possible by a donation from Anelva Corporation (now part of Canon Inc.) of Japan, and consists of a check for US $ 1000 and a citation. We will continue this feature in the Cancun symposium (again facilitated by a donation from the Anelva Corporation, Japan), and will select the best paper on the basis of the quality of both the manuscript and the presentation.

Chapter 1: Electrical Characterization

This chapter contains five papers. The first paper (invited) in this chapter by Wilson et al highlights the recent advances achieved in the non-contact corona-Kelvin measuring technique. This technique yields the V-Q and the C-V characteristics, EOT, the threshold voltage, the flat-band voltage, total dielectric charge, and the interface state density over a large surface potential. The second paper by Xiong et al is an investigation of the work function of TaSiN and TaCN films on HfO₂ or SiO₂ gate dielectrics by a combination of different electrical characterization techniques; the reported results show ~ 0.2 eV work function difference between these two metals, suggesting that Fermi-level pinning is not a problem for these metal systems. The third paper by Avellan et al is an investigation of the deposition pressure and temperature on the trap energy in the HfSiO₃ gate dielectric and the related trap-assisted tunneling current. Results indicate the deposition parameters to change the trap energy by more than 0.3 eV.
The fourth paper by Ota et al has examined the dependence of electron mobility on the Al and N profiles in the HfAlON gate dielectric; the paper reports a strong influence of the N-profile on the mobility, and no significant effect of the Al-profile. The last paper in this chapter by Atarah et al reports that the phonon limited carrier mobility is accurately characterized by an exponential relationship over a wide range of temperature and electric field.

Chapter 2: High Mobility Substrates

This chapter consists of two invited papers. The first paper, by Ye et al discusses the electrical properties of Al₂O₃/InGaAs and Al₂O₃/GaAs based devices. Overall, better device characteristics are observed on InGaAs substrates, with a particularly low density of interface states, in the mid 10¹¹ cm⁻² eV⁻¹ range. The second invited paper, by Kita et al, reviews the physical and electrical properties of Ge-based MOS structures, more specifically comparing Y₂O₃ and HfO₂ deposited on Ge. It is shown that the Ge/Y₂O₃ system shows better interface quality and better thermal stability compared to Ge/HfO₂. These 2 complementary papers present the progress towards high-mobility/high-k devices, with Ge considered as a good substrate candidate for p-channel devices and (In)GaAs for n channel devices.

Chapter 3: Interfaces and Defects

This chapter contains four invited papers and one contributed paper. For high-k based gate stacks, both the substrate/dielectric and the dielectric/gate electrode interface are subject of extensive research, as many of the observed issues and deficiencies can be attributed to interface related problems. It is shown in this section, that the silicon/dielectric interfaces exhibit interface defects that are very similar to conventional SiO₂ oxides, i.e. many of the defects are silicon dangling bonds. These interface defects do have an impact on reliability, NBTI, mobility, and drive currents. Successful passivation of these defects requires higher temperature forming gas anneal or exposure to atomic hydrogen plasma. Also, for Ge (or Ge containing substrates), the effect of surface passivation and control is proven to be key to success. Also, the dielectric/gate electrode interface has an important bearing on the device properties, such as the effective work-function difference (or Vt control). A model is presented, that invokes the selective interface bonding and electronic state density to explain/understand the observed work-functions, especially for PMOS metals.

Chapter 4: Physical/Chemical Characterization

This chapter includes 4 papers. The 1st paper (invited) by Ikarashi et al describes how the chemical composition of a HfₓSi₁₋ₓO₂ film affects the electronic structure near the bandgap, using STEM-EELS and ab initio electronic structure calculations. They show that the bandgap of HF-rich HfₓSi₁₋ₓO₂ (x ≥0.5) is identical to that of HfO₂ whereas that of N-incorporated Hf₀.₅Si₀.₅O₂ (20 atomic % of N) is smaller than that of Hf₀.₅Si₀.₅O₂ film. In the 2nd paper (invited), MacKenzie et al, shows the evidence of interface reactions having occurred with the formation of an oxide layer at the TiN/poly-Si interface of Si(100)/SiO₂/HfO₂/TiN/poly-Si gate stack prior to activation, using electron energy-loss spectroscopy. Analysis of the Si L-edges indicates that this oxide is likely to be an
oxynitride. As a result, the usefulness of EELS spectrum imaging to investigations of interface reactions has been demonstrated.

The 3rd paper, by Conard et al, reports possible modification of the chemical states at the high-k oxide/metal interface. They also showed increase of the nitrogen content in the TaN, interdiffusion of the Ti and TaN, and formation of Ta$_2$O$_5$ at the TaN/HfO$_2$ interface, in the case of the TiN/TaN/HfO$_2$/SiO$_2$/Si stack, upon 1000 $^\circ$C N$_2$ annealing. In the final paper (invited) of this chapter, Miyasaki et al, present in-depth profiling of chemical bonding features and defect state density in ultrathin HfSiO$_x$Ny films, by using x-ray photoelectron spectroscopy (XPS) and total photoelectron yield spectroscopy (PYS) in combination with oxide thinning in a dilute HF solution. The PYS analysis shows that, for the annealed samples, the defect state density increases with the N content and becomes maximum in the oxygen-deficient near-surface region.

**Chapter 5: High-k Materials for Memory**

This chapter consists of two papers. Piagge et al describe the structural/chemical properties of annealed Al$_2$O$_3$ films for interpoly dielectrics in flash memories. The alumina films were deposited by ALD and annealed in ammonia or oxygen to introduce nitrogen, or improve the stoichiometry. The levels of nitrogen attained did not significantly influence the dielectric properties of the film, but did increase the temperature at which the alumina crystallized into the gamma phase due to the formation of AlN bonds. The oxygen anneals retarded the diffusion of nitrogen in the films, probably by saturating the Al bonds and increased the thickness of an interfacial layer. Birge et al described a new floating gate flash memory based on the trapping and detrapping of holes injected from the substrate into an ITO (indium-tin-oxide) layer by tunneling and interpoly oxide layers composed of Zr-doped HfO$_2$. The injected charges displayed excellent long-term retention after 5000 seconds. Further improvements in the memory window and erasing efficiency can be expected from an optimization of the dielectric thickness of the insulator layers.

**Chapter 6: Reliability Issues**

This chapter consists of two invited and four contributed papers. Much of the reliability issues of high-k gate dielectrics remains to be understood and resolved before a complete integration of these materials in future CMOS technologies. The chapter on reliability starts with an invited paper and discusses the threshold voltage instability and low frequency noise in Hafnium-based gate dielectrics. The following two papers discuss the negative bias temperature instability (NBTI) issues in Hf-based gate dielectrics. Two papers then discuss the charge trapping problems and reliability issues in lanthanum oxide and lanthanum silicate respectively, followed by an invited paper about breakdown characteristics of mixed oxide high-k gate dielectrics for memory applications.

**Chapter 7: Modeling**

Two invited papers and three contributed papers are presented in this chapter. The first invited paper, by Fiorentini et al, presents calculations of defect levels in various dielectrics, based on the density functional theory. By properly accounting for self
electronic interactions, it is shown that computations of band gaps and defect levels are coming in good agreement with the experimental results. The second invited paper, by Gavartin et al, is focusing on calculations of polaronic charge trapping in high-k materials. It is found that trapping of electrons at oxygen vacancies in HfO₂ occurs most likely via a polaron-like mechanism, corresponding to the formation of localized defects resulting from the interaction of the electron with the lattice. The next three contributed papers are discussing the following topics: the electronic structure of bulk and defect CaCu₃Ti₄O₁₂ using density functional theory, by Alippi et al, the simulation of trap-assisted tunneling current in high-k gate stacks, by Karner et al, and the modeling of the dielectric response of DyScO₃ and LaAlO₃ using density functional theory, by Delugas et al. In summary, this chapter highlights recent progress achieved in the computation of high-k dielectric properties, mainly using ab-initio calculations, illustrating what insights can be gained from theory.

Chapter 8: Gate Electrode Materials and Processing

This chapter presents six papers. The first paper (invited) by Biswas et al is an investigation of the mechanism of work function tuning in NiₓTa₁₋ₓ and NiₓPt₁₋ₓSi gate electrodes, for NMOS and PMOS applications, respectively. The results indicated the work function change to decrease and the Fermi level pinning to increase with the Hf content in the HfSiOₓ gate dielectric. The second paper by Sugita et al reports adjustment of the work function of TaSiₓNy gate electrodes by varying the composition through alternate deposition of TaN from PDMAT and NH₃ and Si from SiH₄ or Si₂H₆. The third paper (invited) by Green et al is an investigation of the Ni-Ti-Pt ternary alloy as a gate electrode on HfO₂ by the combinatorial methodology. The results suggest smaller work functions near the Ti-rich corner and higher work functions near the Ni- and Pt-rich corners.

The fourth paper (invited) by Ohmori et al describes how a wide range (~1.2 V) in flat-band voltage variation was obtained by changing the composition of a Pt-W alloy as the gate electrode on La₂O₃ gate dielectric; this result highlights an important asset of La₂O₃ as a gate dielectric. The fifth paper (invited) in this chapter is an investigation of the comparative merits of ALD and AVD HfSiOₓ films as gate dielectrics and of TaN, Ru, and RuO₂ as gate electrodes. The last paper in this chapter by Starzynski reports on a superior non-flammable wet etchant for TaC, with good selectivity with respect to HfO₂ and SiO₂, and reasonable etch rates for TaC. This would be most useful in a dual-gate CMOS fabrication process.

Chapter 9: High-K Processing

This chapter contains six papers and starts with an invited paper that gives a comprehensive discussion on materials and processes for high-k gate stacks. The following paper reports on the development of a 300mm MOCVD HfSiOₓ process within a wide composition range and the third paper outlines a processing condition to improve the characteristics of lanthanum oxide. The fourth paper by Kim et al describes an ALD process including ammonia that is used to deposit nitrided Hf oxide films. The CV and JV characteristics indicate that the nitrogen incorporation results in a lower leakage current degradation under constant voltage stress, probably due to the passivation of bulk traps by nitrogen. Dussarrat et al describe the composition of HfSiOₓ films deposited by
ALD using alternate pulses of Hf and Si cation precursor interspersed with pulses of ozone. TDEAH (Hf(NEt₂)₄) and TSA (trisylylamine) bubblers were used for the Hf and Si, respectively and the TSA resulted in very low carbon contamination. The Hf/Si concentration ratio in the films corresponds to that expected from the ratio of the number of Hf to Si pulses. Mole fractions of HfO₂ in the films ranged from 40-100 %. This may be the most controllable way of producing high-quality Hf silicate films described to date. An excellent paper by Lichtenwalner et al describes advances in producing 8” SOI wafers using an ultra high-vacuum growth approach to deposit the epitaxial insulator and semiconductor overlayers. Target thicknesses were 5 nm and 10 nm for the semiconductor (Si, SiGe) and insulator, respectively. The most promising approach used Ca₁₋ₓSrₓTiO₃ as an epitaxial insulator. It was stable to at least 700 °C in vacuum. However, long annealing times in oxygen will be required to ”float” the oxide to increase its equivalent thickness and reduce capacitive coupling.

Chapter 10: High-k Materials

This chapter consists of three invited and three contributed papers. Although the quest for replacement of SiO₂ based dielectrics has been focusing in recent years on Hf-based dielectrics, there seems to be a renewed interest in alternative dielectric materials. In this section intriguing results are presented on Zr, and rare earth (Dy, Sc, La, Ce, ...) containing dielectrics. Addition of Zr to Hf based dielectrics is shown to stabilize the tetragonal crystalline phase, results in smaller grains, more uniform leakage current distributions, and reliability. Also rare earth containing dielectrics are demonstrated to exhibit good dielectric constants (k~ 15-25) and potential to scale well below 1.0 nm EOT (with moderate thermal budgets). Understanding and control of interface reactions between these rare-earth dielectrics and Si (or SiO₂) interfaces is a key research area, addressed in many of the contributed papers in this section.

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