Integration and frequency dependent parametric modeling of Through Silicon Via involved in high density 3D chip stacking

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Evaluation of Through Silicon Via (TSV) electrical performance is hardly required today to improve heterogeneous 3D chip performance in the frame of a “more than Moore” approach. Accurate modeling of TSV is consequently essential to perform design optimizations and process tuning. This paper proposes a methodology based on RF characterizations and simulations, leading to a frequency dependent analytical model including MOS effect of high aspect ratio TSV. Specific test structures integrated on both floating Si bulk and CMOS 65 nm active wafers according to a face-to-face Via Last After Bonding process enable C(V) and RF measurements. TSV equivalent model including all substrate effects is proposed according to CMOS 65 nm specificities (voltage, frequency, dimensions and Si conductivity) and implemented in SPICE simulator to predict TSV impact on signal propagation.

Introduction

2D ICs limitations haled recently microelectronic manufacturers to pick up an “out of the box” way of thinking, to explore solutions beyond standard Moore’s law. Thus, a “More Moore” approach proposes to gather lots of functions from a same technological node while carrying on an integration density increase. The other alternative consists in following a “More Than Moore” path, assembling heterogeneous dies from mature technologies [1]. Fig. 1 sets 3D integration halfway between SiP and SoC, in the frame of both More Moore and More than Moore approach. This brand new technology is a real new paradigm in microelectronics and seems to be the perfect candidate to overcome standard 2D ICs limitations. It is indeed expected to improve circuit electrical performance like RC delay [2, 3], reduce chip weight [4, 5] and power consumption, and opens new perspectives in term of heterogeneous integration enabling more sophisticated than ever system on chip integration. Today, 3D is a young technology with lots of possible integration schemes and challenges to take up.
Overview of 3D Process Flows

Several 3D approaches featuring different TSV densities, different materials and lots of key technology coexist today providing manufacturers a large choice of integration schemes. The following parts give an overview of the common stacking techniques frequently employed.

First we have to distinguish between collective bonding and single die processing techniques. Indeed, single chip can be stacked over another one in a die to die approach (D2D [6]) or over a wafer according to a die to wafer method (D2W [7, 8]). Wafer to wafer bonding (W2W [9]) can be performed too, leading to a collective stacking of the whole embedded dies. Although W2W approach provides the highest production throughput and alignment accuracy, stacked dies must have the same size, reducing modular aspect of 3D integration, and potential non-functional dies from two wafers are heaped which hardly restricts final yield. In a D2D or D2W approach, if functional test are performed before stacking, only KGD are processed increasing final yield. However, regarding low alignment accuracy and velocity provided by stacking tools, throughputs of these two techniques are lower than for a collective bonding approach.

Whatever the integration scheme, the same key technologies are achieved to perform 3D stacks. It includes wafer bonding and thinning, TSV etching, isolation and filling. The sequence of these steps will lead to a “via first”, “via middle”, “via last” or “via last after bonding” approach whether TSV is integrated respectively before the FEOL, after the FEOL and before the BEOL, after the BEOL or after bonding. Fig. 2 shows an overview of all these techniques. Many integration options are consequently available and the final product is the main driver to choose the best technological solution.

3D integration is expected to improve stack performance and replace long high inductive and capacitive wire bonds by short vertical interconnects whose density is between $10^2$ and $10^5$ TSV/mm$^2$. Typically, if only few basic signals are transmitted, medium density TSV ($\approx 100$ to 1000/mm$^2$) are sufficient to ensure communication between stacked dies. These vias are generally partially filled and feature a low aspect ratio (1 or 2) and TSV diameter $\approx 100$ µm. They are integrated instead of wire bonds.
usually involved in SiP chips like stacked memories [10], image sensors [11, 12], MEMS [13], or embedded in silicon interposer [14]. On the other hand, the transmission of a wide range of signals on a large broadband requires high density TSV (Stacked ICs technology, or 3D SiC), fully filled and featuring high aspect ratios (5 to 20) and TSV diameter ≈ 1 to 10 μm. For instance, 3D SiC TSV are frequently observed in memory on logic stacks, in 3D System On Chips (SoC) and in the future, these vias are expected to connect dies and functional blocs inside complex heterogeneous stacking.

Figure 2: Comparison of main TSV integration flows [15]

Whatever the process flow TSV remains the nerve centre of the stack and have to transmit a wide range of signals (analog, digital, RF etc.) on a large broadband. It’s consequently hardly required to model TSV, evaluate its performance and make sure that it is in good agreement with customer specifications.

Overview of TSV modeling techniques

Several authors have recently developed tools and models to predict TSV behavior from measurements, simulations or empirical calculations. They provide RC analytical models [16], high frequency RLCG models [17-19] and compact models [20]. In this way, in 2005 a TSV model built from RF measurements was proposed by Leung et al. for 400 μm deep and 50 to 70 μm wide TSV integrated on high resistivity substrates [17]. This tentative (Fig. 3) enables to extract TSV resistance $R_c(f)$, inductance $L_c(f)$ and dielectric losses $R_{sub}(f)$ including frequency dependent phenomenon.

Figure 3: TSV electrical model proposed by Leung et al. [17].
Empirical analytical expressions of these three elements including experimental fitting parameters were built from extracted values. They are all frequency dependent following a $\sqrt{F}$ trend depicting skin effect occurring in high frequencies. In 2006, Ryu et al. proposed another TSV equivalent model extracted from RF measurements [18] (Fig. 4). 75 μm wide and 90 μm deep TSV were integrated on standard Si substrates ($\rho = 10 \ \Omega \cdot \text{cm}$) usually processed in CMOS technology. The model includes TSV resistance $R_{\text{via}}$, inductance $L_{\text{via}}$, capacitance $C_{\text{ox, via}}$ due to isolation oxide between TSV and silicon, oxide capacitance between TSV $C_{\text{ox}}$, and substrate losses ($C_{\text{Si}}$ and $G_{\text{Si}}$). It enables to extract TSV performance including crosstalk and empirical model of TSV resistance is put forward.

![TSV electrical model proposed by Ryu et al [18].](image)

**Figure 4**: TSV electrical model proposed by Ryu et al [18].

Finally, MOS effect has been recently considered in other publications [21-24] to make TSV model as accurate as possible whatever the bias voltage and substrate polarization.

**Methodology for TSV modeling**

In this paper, a full methodology to accurately predict TSV performance is proposed (Fig. 5). TSV electrical model is extracted from both RF measurements and electromagnetic (EM) simulations and gives link between via electrical performance and technological parameters through analytical expressions.

First, this methodology is implemented for TSV integrated on floating Si substrate. Integration process leading to face to face via last after bonding stacks is detailed. Specific structures using this flow are then considered for RF characterizations and EM simulations (Ansoft – HFSS) and TSV equivalent model is proposed. HFSS simulator previously validated as a predictive tool enables to perform simulations in the frame of a design of experiments (DOE) leading to analytical model for each model parameter. In order to evaluate the impact of substrate polarization on signal transmission, TSV structures are integrated onto a CMOS 65 wafer and characterized. $C(V)$ and RF measurements are achieved and enable to improve TSV model considering depletion effect in Si bulk. This equivalent model is helpful for design and technological recommendations and TSV impact on 3D ring oscillators can be evaluated through SPICE simulations, as shown in the last part.
In order to build such an electrical model, specific test structures are required to validate the methodology first step (Fig. 5). Thus, high density TSV integration process and dedicated devices for RF and C(V) measurements are presented below.

High density TSV integration

In this part a full process flow enabling 3D integration is detailed. Wafer stacking is achieved in a face to face via last after bonding approach including high density cylindrical TSV (~10^4 TSV/mm^2).

First, surfaces of both top wafer and Si substrate are prepared with a chemical and mechanical polishing (CMP) and cleaning. A face-to-face stacking is performed with direct oxide bonding, providing efficient and durable cohesion. The stack is then thinned down to 15 μm by a combination of grinding and CMP steps. After thinning, total thickness variation (TTV) and roughness are respectively 1 μm and 0.5 nm RMS. A final stress release step enables to reduce wafer bow down to 20 μm. It is hardly required to minimize TTV, roughness and bow to ensure good conditions for TSV photolithography and patterning. After bonding and thinning, a 1 μm oxide layer is deposited by PECVD to ensure the electrical insulation of future TSV and Redistribution Layer (RDL).

Once 3 μm wide TSV are patterned by lithography [25], dielectric top layer, thin Si substrate and Pre Metal Dielectric (PMD) are etched with successive Reactive Ion Etching (DRIE) process steps, using respectively (C_4F_8, O_2) mix for dielectric and (SF_6,
C₄F₈) for silicon. Straight etching profile is required to ensure good step coverage during metallization and to limit charge trapping at Si/SiO₂ interface. Gas mixes enable to minimize scalloping effect on TSV sidewalls and low scalloping undercut were measured (respectively less than 30 and 50 nm). PMD oxide, enabling isolation between M1 and substrate, is partially etched in order to prevent copper line from oxidation during stripping and isolation processes.

After stripping, efficient cleaning is mandatory to ensure removal of etching residues and promote a good adhesion of isolation layer on TSV sidewalls. Then a 400 nm thick SiO₂ layer is deposited by Sub-Atmospheric Chemical Vapor Deposition (SACVD) in order to insulate TSV from the substrate. This technique enables a high conformity (300 nm is measured on TSV sidewalls) and good step coverage (70%). An etch back process is finally used to remove bottom oxide and open TSV on metal line M1. Then a 20 nm TiN barrier is deposited by Metal-Organic Chemical Vapor Deposition (MOCVD) as copper diffusion barrier, followed by deposition of a 200 nm thick copper seed layer. This last step consists in two successive depositions of 50 nm PVD (Physical Vapor Deposition) and 150 nm CVD copper layers. The first film ensures Cu adhesion on diffusion barrier but shows a lack of continuity on TSV sidewalls. Conformal CVD film is thereby deposited to ensure a sufficient seed layer for the subsequent copper electrolytic deposition (ECD). To complete metallization, TSV are filled by ECD and annealed at 250°C during 1 hour. Electrolyte and process tuning provide dense copper and voidless TSV as shown on Fig. 6. To make test structure functional, RDL is finally added to connect TSV according to a standard Damascene process. As shown on Fig. 6, the oxide layer is conformal, and a good contact between TSV and M1 can be observed whereas no etching residue remains.

Figure 6: SEM cross section of a TSV after filling

TSV electrical modeling

In order to accurately characterize TSV, specific RF structures are integrated on floating Si substrate according to the integration process previously described. RF Dispositive Under Test (DUT) is a TSV dual chain including two high density TSV with coplanar ground lines and GSG RF pads. Fig. 7 show X-ray tomography picture of TSV chains dedicated to RF characterizations, including high density TSV.
Figure 7: X-ray tomography picture of a TSV dual chain designed for RF characterizations

TSV characterization and modeling

RF measurements, PI shaped model extraction and simulator validation

After a calibration step DUT scattering parameters [S] are measured using an Anritsu 37397C Vector Network Analyser (VNA). A deembedding [26] followed by a calculation step based on a π shaped equivalent model enables to transform measured [S] of the chain into TSV dual chain RLCG parameters, as shown in Fig. 8a. Besides, 10 μm long intervia line between the two TSV is modelled as an RL equivalent circuit. Its resistance (R\text{line}) and inductance (L\text{line}) are simulated being constant with frequency: \( R\text{line} = 10 \, \text{mΩ} \cdot \mu\text{m}^{-1} \) and \( L\text{line} = 0.7 \, \text{pH} \cdot \mu\text{m}^{-1} \). A last calculation step enables to extract single TSV intrinsic RLCG parameters removing the effect of this intervia line (Fig. 8b).

Figure 8: DUT PI model and TSV PI equivalent model

Same structures are simulated using the Ansoft HFSS 3D full wave simulator. Simulated RLCG parameters are extracted according to the same methodology previously presented for RF measurements. Measured and simulated TSV RLCG parameters are compared in Fig. 9.

According to Fig. 9a, measured and simulated TSV resistance increase with frequency due to skin effect and simulation fits in an excellent way measured R parameter whatever the frequency. Extracted resistance value at low frequency (\( R = 150 \, \text{mΩ} \)) is in good agreement with static R measurements performed on Kelvin structures, and it increases up to 200 mΩ at 20 GHz.
Figure 9: Evolution of measured and simulated TSV resistance (a), inductance (b), capacitance (c) and conductance (d) with frequency

Fig. 9b shows the good agreement between simulations and measurements for TSV inductance. In spite of the small increase for lower frequencies, L is assessed to be constant with frequency. Such very low value (L measured ≈ 5 pH) makes TSV inductance about 500 times lower than conventional wire bonding. Finally, simulated capacitance fits in a perfect way the measurements (Fig. 9c) and according to Fig. 9d results are in good accordance for TSV conductance in spite of the noise due to the low values of measured parasitic elements. These agreements observed for the whole electrical parameters of TSV make the simulator able to predict the via behavior as a function of frequency. However, in order to extract intrinsic parasitic elements of the TSV and explain the complex frequency dependent evolution of C and G, it is necessary to turn the first equivalent model into a more physical one.

TSV physical model

In this enhanced model (Fig. 10) C_{ox} represents oxide capacitance between TSV and silicon due to isolation oxide. G_{Si} and C_{Si} are parasitic elements due to presence of lossy silicon substrate. The frequency dependent evolution of C and G is consequently caused by the combination of these three elements.
Impedance identification between \((C, G)\) and \((C_{Si}, G_{Si}, C_{ox})\) gives equations eq.1 and eq.2 enabling to switch between both models.

\[
C = \frac{C_{ox}}{G_{si}^2 + \omega^2(C_{si} + C_{ox})^2 + \omega^2(C_{si} + C_{ox})^2}
\]

\[
G = \frac{G_{si}C_{ox}^2 \omega^2}{G_{si}^2 + \omega^2(C_{si} + C_{ox})^2}
\]

At low frequencies, eq. 1 becomes eq. 3 and it is possible to extract oxide capacitance from measurements or simulations. On the other hand, in high frequencies, eq. 1 becomes eq. 4 and \(C_{Si}\) can finally be extracted from measurements.

\[
\lim_{\omega \to 0} C = C_{ox}
\]

\[
\lim_{\omega \to \infty} C = \frac{C_{ox} C_{si}}{C_{ox} + C_{si}} = C_{\infty}
\]

In the same way, \(G_{Si}\) is expected to be constant and represents with \(C_{Si}\) conduction losses in Si substrate. It is extracted considering the limit of eq. 2 in high frequencies (eq. 5).

\[
\lim_{\omega \to \infty} G = \frac{C_{ox}^2 G_{si}}{(C_{ox} + C_{si})^2} = G_{\infty}
\]

According to eq. 3, 4 and 5, via parasitic elements are extracted and all the electrical performance of this high density TSV whose integration process was presented previously are summarized in table 1. Low inductance and capacitance values make TSV performance about 500 times better than conventional wire bonding one. It could be consequently an excellent candidate to overcome 2D ICs limitations.
TABLE I. High density TSV electrical performance

<table>
<thead>
<tr>
<th>Electrical parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{dc} (mΩ)</td>
<td>150 (skin effect at high frequency)</td>
</tr>
<tr>
<td>L (pH)</td>
<td>4</td>
</tr>
<tr>
<td>C_{ox} (fF)</td>
<td>40</td>
</tr>
<tr>
<td>C_{Si} (fF)</td>
<td>7</td>
</tr>
<tr>
<td>G_{Si} (mS)</td>
<td>0.4</td>
</tr>
</tbody>
</table>

TSV analytical model and predictive simulations

To model and predict TSV performance whatever the materials and the geometry, accurate links have to be identified between electrical parameters and TSV characteristics. TSV resistance and oxide capacitance models have already been validated and physical models are proposed in eq. 6 and eq. 7.

\[ R = R_{Barrier} + \frac{\rho_{Cu} \cdot t_{Si}}{\pi \cdot (D_{TSV} \cdot \delta - \delta^2)} \]  

\[ C_{ox} = \frac{2 \cdot \pi \cdot \varepsilon_0 \cdot \varepsilon_{dil} \cdot t_{Si}}{\ln \left( \frac{0.5D_{TSV}}{0.5D_{TSV} - t_{dil}} \right)} \]  

\( t_{Si} \) is TSV depth, \( \rho_{Cu} \) copper resistivity, \( \varepsilon_{Si} \) silicon permittivity, \( \varepsilon_{dil} \) oxide permittivity and \( D_{TSV} \) TSV diameter. TSV resistance model is made of two main elements: the first one represents diffusion barrier resistance, and the second one TSV copper resistance, including skin effect through frequency dependent skin depth (\( \delta \)). Oxide capacitance basically depends on dielectric thickness and permittivity, and TSV dimensions. However, no physical model being available for TSV inductance \( L \), \( C_{Si} \) and \( G_{Si} \), a design of experiments (DOE) using the previously calibrated Ansoft HFSS simulator is carried out to model these elements as functions of three main factors (TSV diameter (\( D_{TSV} \)), TSV depth (\( t_{Si} \)) and silicon conductivity (\( \sigma_{Si} \)) capable to affect these response variables. Their domains are given in table II.

TABLE II. Factor domains

<table>
<thead>
<tr>
<th>DOE factor</th>
<th>Lowest value</th>
<th>Highest value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \sigma_{Si} ) (S/m)</td>
<td>1</td>
<td>100</td>
</tr>
<tr>
<td>t_{Si} (μm)</td>
<td>10</td>
<td>50</td>
</tr>
<tr>
<td>D_{TSV} (μm)</td>
<td>2</td>
<td>10</td>
</tr>
</tbody>
</table>

The excellent fit between simulations and DOE prediction demonstrates that resulting analytical expressions are able to reproduce variations observed during EM simulations. Finally, to give a physical sense to modelled responses and make them easier to use, DOE quadratic expressions are transformed using the expression given in [20]. Eq. 8, 9 and 10 show the final semi-empirical expressions of TSV inductance, \( C_{Si} \) and \( G_{Si} \).

\[ L = \mu_0 \cdot t_{Si} \cdot 0.22 \cdot \ln \left( 1 + 0.33 \frac{t_{Si}}{D_{TSV}} \right) \]
The TSV analytical model (Eq. 6 – 10) is finally validated in the frame of a comparison with RF measurements. Fig. 11a and 11b show how eq. 6 and 8 fit measured TSV inductance and resistance, while eq. 1 and 2 enable to reconstitute C and G behavior and consequently validate $C_{ox}$, $C_{Si}$ and $G_{Si}$ models (Fig. 11c and 11d).

\[
C_{Si} = \frac{3 \sigma_{Si}^{0.5} \varepsilon_0 \varepsilon_{Si} t_{Si}}{LN\left(1 + \frac{t_{Si}}{D_{TSV}}\right)}
\]  \tag{11}

\[
G_{Si} = \frac{C_{Si} \sigma_{Si}}{\varepsilon_0 \varepsilon_{Si}} = \frac{3 \sigma_{Si}^{1.3} t_{Si}}{LN\left(1 + \frac{t_{Si}}{D_{TSV}}\right)}
\]  \tag{12}

The excellent agreements presented on these pictures show that analytical models are able to reproduce TSV electrical behavior with technological inputs. These equations are now available for predictive calculations, process tuning and technological recommendations.

Technological recommendations

Another DOE is performed to draw Pareto chart of each analytical expression of TSV model as a function of all geometrical and process parameters. These charts show each of the estimated effects and interactions from the more to the less important factor on
modelled response. It reveals that, as expected, $\sigma_{Si}$ is the most influential parameter on $C_{Si}$ and $G_{Si}$, that TSV resistance is mostly impacted by via diameter, inductance hardly depends on TSV depth and dielectric thickness has the most important effect on oxide capacitance. Fig. 12 shows pie charts that summarize main effect on TSV resistance and inductance.

![Pie chart showing parameter impact on TSV resistance and inductance](image)

**Figure 12**: Sensitivity study: TSV model parameter impact on TSV resistance (a) and inductance (b)

Although TSV diameter is the most influential parameter for TSV resistance, its impact on inductance is low compared to TSV depth. The analytical expressions are consequently helpful to make trade off and to know what parameters have to be adjusted for electrical performance tuning.

**Effect of substrate polarization**

**Structure description**

In order to investigate the impact of substrate polarization on TSV equivalent model and electrical performance, new TSV RF structures are integrated on a CMOS 65 bottom wafer according to the process presented previously (Fig. 13a). C(V) devices including a single TSV surrounded by a ground ring at M1 level are integrated, enabling the study of the MOS capacitance behavior of the via (Fig. 13b). TSV dual chain RF structures are built in too, including substrate contacts to add DC bias to RF signal (Fig. 14)

![Schematic view and SEM cross section of high density TSV integrated over CMOS 65 wafer](image)

**Figure 13**: Schematic view (a) and SEM cross section (b) of high density TSV integrated over CMOS 65 wafer
Impact of Si polarization on electrical performance

RF measurements are performed with a VNA on TSV chains from 0 to 10 GHz with substrate polarization $V_g$ added to RF signal. The methodology (Fig. 5) enables to extract and model $R$ and $L$. According to Fig. 15a and 15b, analytical models proposed in modeling section are still in excellent agreement with RF measurements for $R$ and $L$ in spite of the polarization. Besides DC bias has no impact on these two parameters and each TSV exhibits a static resistance of 170 mΩ and an inductance of $L = 4$ pH whatever the $V_g$ value.

Concerning TSV capacitance, for $V_g = -20$ V (Electric field $E = 1.33$ MV/cm - Fig. 16a), $C$ evolution is the same than without polarization and the methodology is used to extract $C_{ox} \sim 40$ fF from global $C_{TSV}$ at low frequency. $C_{ox}$ expression (eq. 7) gives $C_{ox} = 38$ fF. In the same way, $C_{Si}$ is extracted at high frequency and $C_{Si} \sim 5$ fF. Previous $C_{si}$ model (eq. 9) is obsolete since substrate is now connected to the ground. As a consequence, $C_{si}$ is modelled with eq. 11 giving $C_{si} = 5$ fF. Proposed analytical model fits in an excellent way experimental data.

$$C_{si} = 2 \cdot \pi \cdot \varepsilon_0 \cdot \varepsilon_{si} \cdot t_{si} / \ln\left( R_{ring} / R_{TSV} \right)$$  (11)
Where \( R_{ring} \) is the distance to the nearest ground plane. Finally, \( G_{Si} \) is extracted from \( G_{TSV} \) measurement in high frequency and \( G_{Si} = 0.47 \, \text{mS} \) (Fig. 17). As \( C_{Si} \) et \( G_{Si} \) still stand for conduction losses in Si bulk, \( G_{Si} \) can be calculated according to eq. 10 and \( G_{Si} = 0.47 \, \text{mS} \), fitting extracted value in a perfect way.

![Figure 16: Evolution of global TSV capacitance with negative bias voltage (a) and positive bias voltage (b)](image1)

![Figure 17: Evolution of global TSV capacitance with negative bias voltage (a) and positive bias voltage (b)](image2)

However, if \( V_g +20 \, \text{V} \), \( C(f) \) curve do no longer have the same shape (Fig. 16b) demonstrating that TSV capacitance is a combination of \( C_{ox} \) and another electrical element. An impact of the TSV bias is observed on \( G_{Si} \) as it is denoted for TSV capacitance. A depletion capacitance is consequently incorporated into a new model (Fig. 18) to reproduce the TSV behavior as a function of bias voltage. The next part aims at modelling and evaluating this new parameter.

![Figure 18: High density TSV model with polarized substrate](image3)
C(V) measurements and depletion capacitance modeling

Fig. 19a shows theoretical C(V) characteristic for p-type substrates. In the accumulation region, where TSV voltage \( (V_g) \) is lower than flat band voltage \( (V_{FB}) \), oxide capacitance can be extracted. In the inversion region \( (V_g > \text{threshold voltage (Vth)}) \), C(V) curve is expected to follow the high frequency line regarding AC component signal frequency usually sent through TSV. 25-TSV matrices are measured to plot C(V) characteristics. Fig. 19b shows a C(V) curve at 300 kHz, and \( C_{ox} \sim 36 \text{ fF} \). An important shift in the negative \( V_g \) values and distortions of the curve mainly due to high charge density at the TSV Si/SiO\(_2\) interface \( Q_{SS} \) [24] are observed in spite of process tuning. In depletion region (Fig. 4), the capacitance does not follow « high frequency » curve because of interface charges and the too low measurement frequency enabling a weak inversion layer to settle.

![Figure 19](image)

**Figure 19**: Theoretical C(V) curve (a) and high density TSV C(V) measurement plot

Depletion effect observed on C(V) measurements can be modelled based on [21] and adding the polarization due to charge trapping at the Si/SiO\(_2\) interface caused by etching process and dielectric deposition. TSV voltage \( (V_g) \) and resulting flat band voltage \( (V_{FB}) \) are given by eq. 12 and eq. 13.

\[
V_g = V_{FB} + V_S + \frac{Q_M}{C_{ox}} \quad (12)
\]

\[
V_{FB} = \phi_M - \phi_S - \frac{Q_{SS} \cdot q \cdot S}{C_{ox}} \quad (13)
\]

\( C_{ox} \) is the oxide capacitance, \( Q_M \) is the electronic charge on metal, \( \phi_M \) and \( \phi_S \) are metal and semiconductor work functions respectively, \( q = 1,6.10^{-19} \text{ C} \), \( S \) is contact surface between Si bulk and oxide and \( V_s \) is Si surface potential. Eq. 13 and eq. 7 give eq. 14.

\[
V_{FB} = \phi_M - \phi_S - \frac{Q_{SS} \cdot q \cdot R}{\varepsilon_0 \cdot \varepsilon_{ox}} \cdot \ln \left( \frac{R}{R - t_{ox}} \right) \quad (14)
\]

Analytical depletion capacitance expression \( (C_{dep}) \) is obtained by solving cylindrical Poisson’s equation, assuming that longitudinal and peripheral potential variations are negligible. Consequently, 1D equation (eq.15) is sufficient to describe potential
evolution in Si bulk surrounding TSV. Moreover the depletion approximation (for \( R \leq r \leq R_D \), where \( R_D = R_{TSV} + W_{depletion} \)) (Fig. 20) leads to a depletion charge only due to ionized doping atoms and eq. 15 gives eq. 16.

\[
\Delta V = -\frac{\rho}{\varepsilon_0\varepsilon_{Si}}
\]  
(15)

\[
\frac{1}{r} \frac{\partial}{\partial r} \left( r \frac{\partial V}{\partial r} \right) = \frac{q \cdot N_a}{\varepsilon_0\varepsilon_{Si}}
\]  
(16)

\( N_a \) is the doping concentration of p-substrate (~1.3.10\(^{15}\) at.cm\(^{-3}\) in our case) and \( \varepsilon_{Si} \) is silicon permittivity. The boundary conditions make electric field and potential \( V \) null beyond depletion radius. Two successive integrations are achieved and give \( V_s \):

\[
V_s = \frac{q \cdot N_a}{2 \cdot \varepsilon_0 \cdot \varepsilon_{Si}} \left[ R_D^2 \cdot \ln \left( \frac{R_D}{R} \right) - \left( \frac{R_D^2 - R^2}{2} \right) \right]
\]  
(17)

\[ \text{Figure 20: High density TSV model with polarized substrate} \]

At threshold \( V_s = 2 \cdot \Phi_F \) (eq. 18), and in this case \( V_g = V_{th} \).

\[
V_s = 2 \cdot \phi_F = 2 \cdot \frac{K \cdot T}{q} \ln \left( \frac{N_a}{n_i} \right)
\]  
(18)

Eq. 17 and eq. 18 give eq. 19

\[
2 \cdot \frac{K \cdot T}{q} \ln \left( \frac{N_a}{n_i} \right) = V_s = \frac{q \cdot N_a}{2 \cdot \varepsilon_0 \cdot \varepsilon_{Si}} \left[ R_{D,\text{max}}^2 \cdot \ln \left( \frac{R_{D,\text{max}}}{R} \right) - \left( \frac{R_{D,\text{max}}^2 - R^2}{2} \right) \right]
\]  
(19)

Considering a high amount of interface charges (\( Q_{ss} = 5.10^{11} \) at.cm\(^{-2}\)), threshold voltage is calculated and \( V_{th} = -5.2 \) V, which is in good agreement with experimental threshold voltage observed on Fig. 19b. In this region, depletion radius does not increase anymore and is noted \( R_{D,\text{max}} \). Using eq. 19, numerical resolution enables to extract maximum depletion radius: \( R_{D,\text{max}} \approx 2.5 \) \( \mu \)m. \( C_{dep} \) is calculated according to eq. 20 and \( C_{dep} = 30 \) fF.
In order to evaluate the impact of a TSV on circuit performance, specific structures are designed and simulated with a SPICE simulator in time domain. Unloaded inverter chain performance are compared to inverters (65 nm node) loaded by a single TSV or by a TSV chain including a 10 μm long RDL (Fig. 21a and 21b).

**Figure 21**: Chained inverters including single TSV (a) and TSV chain (b)

These structures include 4 μm wide and 15 μm deep TSV with 300 nm thick isolation oxide. Electrical performance is extracted thanks to the methodology presented in the previous part and summarized in table III. Besides, RDL line included in TSV chain are simulated and its performance are presented in table IV.

**TABLE III.** TSV nominal electric performance

<table>
<thead>
<tr>
<th>Electrical parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R (mΩ)</td>
<td>72</td>
</tr>
<tr>
<td>L (pH)</td>
<td>3.5</td>
</tr>
<tr>
<td>C_{ox} (fF)</td>
<td>25</td>
</tr>
<tr>
<td>C_{Si} (fF)</td>
<td>7</td>
</tr>
<tr>
<td>G_{Si} (mS)</td>
<td>0.48</td>
</tr>
<tr>
<td>C_{Dep} (fF)</td>
<td>30</td>
</tr>
</tbody>
</table>

**TABLE IV.** RDL line electric performance

<table>
<thead>
<tr>
<th>Electrical parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R (mΩ)</td>
<td>61</td>
</tr>
<tr>
<td>L (pH)</td>
<td>5.12</td>
</tr>
<tr>
<td>C (fF)</td>
<td>10</td>
</tr>
<tr>
<td>G (mS)</td>
<td>2.9e⁻³</td>
</tr>
</tbody>
</table>

Timing analysis is performed and delay time between TSV input and output drivers as well as fall time T_f of signal transmitted in TSV are extracted (Fig. 22). This last parameter gives helpful indications about maximal operating frequency achievable with TSV (F_{max} = (4 T_f)⁻¹). This study is performed for three inverters sizes called X2, X18 and X53 (inverter width respectively 2, 18 and 53 times higher than its length).
Figure 22: Delay time and fall time measured in chained inverters

Fig. 23 presents inverter delay times for the different considered structures.

The first series called “Ref” shows intrinsic inverter delay times for a standard 2D structure. Considered gates exhibit values around 13 ps. The implementation of TSV or TSV chain leads to an increase of delay all the more high as inverter is small. RC additional delay is indeed caused by the time needed to load TSV oxide capacitance. Small drivers (like X2) are slow and not adapted to load such capacitances and consequently are more impacted by the addition of TSV. However, the integration of stronger driver enables to restore timing responses. For example X53 gate delay increases only from 13 ps to 30 ps (from the reference structure to the TSV chain one), limiting effect of the TSV.

In order to evaluate the impact of each element of TSV model on circuit performance, a sensitivity study is carried out for the structures presented on Fig. 21a and b. Electrical parameters of TSV model are successively set at a minimal or maximal value (+/- 30% of the nominal data shown in Table III) and impact on delay time is evaluated for three inverter sizes as shown on Fig. 24 and 25.
As the charts suggest, R, L and C_{Si} have no effect on circuit performance. Indeed, internal input inverter resistance is far higher than TSV one. Optimization and process tuning to reduce resistance or skin effect is consequently pointless regarding delay. G_{Si} has a small impact while C_{ox} and C_{dep} are both critical for delay. For instance, a 30% increase of one of these two capacitances leads to degradation of the delay of 10%. The same trends are observed for fall time. Fig. 25 shows that delay sensitivity to C_{ox}, C_{dep} and G_{Si} is reduced when intervia line is added.

Finally, as it was proposed previously, integration of strong drivers seems to be the best solution to restore time response and limit performance degradation induced by TSV. Process optimization should focus on C_{ox} reduction by thickening the oxide or reducing its k-value.

**Conclusion**

A process flow to perform 3D-IC stacking including high density TSV according to a face-to-face Via Last after bonding approach is presented. A full methodology including RF measurements on both floating and polarized substrate, EM simulations and C(V) measurements is detailed and leads to an accurate analytical model for TSV featuring C_{dep} and bulk conduction losses. This model is available for all technology nodes and enables to extract TSV performance by tuning parameters such as bulk conductivity.
Finally, SPICE simulations enable to identify the most critical parameters in TSV electrical model. $C_{ox}$ and $C_{dep}$ have the highest impact on gate delay and have to be minimized to ensure fast signal transmission, whereas TSV resistance and inductance do not impact inverter delay.

Acknowledgements

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References


15. Yole Développement, *Via First vs. Via Last? The first study to understand 3D integration scenarios*, Final Report -December 2009


