An Overview of Patterned Metal /Dielectric Surface Bonding: Mechanism, Alignment and Characterization

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An overview of the different metal bonding techniques used for 3D integration is presented. Key parameters such as surface preparation, temperature and duration of annealing, achievable wafer-to-wafer alignment and electrical results are reviewed. A special focus is given on direct bonding of patterned metal/dielectric surfaces. A mechanism for copper direct bonding is proposed based on bonding toughness measurements, SAM, XRR, XRD and TEM analysis. Dedicated characterization techniques for such bonding are presented.

Introduction

Bonding of metal surfaces is extensively used for MEMS sealing, power devices, heat dissipation or 3D interconnections. For these applications, techniques such as thermo compression, with or without eutectic alloys or adhesives layers, bumps with low temperature solders or direct bonding are extensively implemented techniques [1-7]. Moreover, for More Moore and More than Moore applications, low temperature bonding and metal bonding are becoming the main drivers of the latest developments. As copper is the main metal used for CMOS interconnects, a high-density Cu interconnection between layer structures, is expected for future three-dimensional integration of electronic devices fabricated on the basis of different technology/design concepts. In this paper, an overview of the different metal bonding techniques used for 3D integration is presented. Key parameters such as surface preparation, temperature and duration of annealing, achievable alignment and electrical results are reviewed. A special focus is done on direct bonding of patterned metal/dielectric surfaces. A mechanism for copper direct bonding is proposed based on bonding toughness measurements, SAM, XRR, XRD and TEM analysis. Dedicated characterization techniques for such bonding are presented.

Hybridization techniques review

Copper is the most (compared to other possible bonding metals) promising candidate for 3D integration technology either for TSV filling or interstate hybridizing. The main reasons of this choice are the wide use of copper in semiconductor device industries and the cost of ownership. On the other hand, the choice of the metal bonding technique is still an open question. Bonding anneal temperature, duration of the annealing, need of an underfill, size and pitch of the interconnect pads, availability of the technique for wafer bonding or die bonding are key parameters in the final choice. Most metallic bonding techniques can be divided into two groups: with and with out thermal compression.
**Bonding with a compression force: diffusion bonding**

The thermal compression bonding is a well-known technique [9,10]. Wafers or dies are pressed together with a controlled force in a bonding tool, while heating is applied (400°C) to allow the bonding diffusion mechanism as shown in Figure 1. Thanks to the compression force, the surfaces roughness is not a limiting factor as the surface asperities are deformed at the bonding interface, therefore surfaces with a roughness in the range of 5 nm can be used. Copper oxide should be avoided or removed right before the bonding process to enable the diffusion of copper. Typically, cleaning of copper surfaces using HCl or acetic acid solutions is performed.

![Figure 1: Different bonding schemes used for thermo compression technique: a) Basic thermocompression (with or without glue between the pads), the temperature is around 400°C, b) Same process but copper-tin alloy is used to decrease the temperature of the process to 250/300°C, c) Hybrid bonding; The compression in the metal pad is induced by the temperature and the high strength of the oxide/oxide bonding part [11]](https://example.com/figure1)

In this technique, for copper bonding, the anneal temperature is difficult to decrease as it monitors the diffusion mechanism and 300°C to 400°C are typical values. Since copper pads do not stick to each other at room temperature with thermocompression, glue is frequently added such as polymers [12,14]. In that particular case the bonding (die to wafer) is facilitated by the polymer and the anneal is applied on all the dies at the same time. IMEC have recently published electrically good yielding of 10k through-wafer 3D via chains with a pitch of 10μm for a via diameter of 5μm [12,13]. For wafer to wafer bonding, Sematech recently has presented submicronic alignment results on 300 mm wafer with 400°C thermocompression bonding [15].

To decrease the anneal temperature, the use of a solder metal at the interface was studied. In the Solid-Liquid Inter-diffusion Bonding (SLID) [16] tin is added on top of one or both of the copper pads. During the anneal at a temperature as low as to 210°C (slightly lower than the tin melting point), intermetallic phases are created. For die to die bonding with copper tin alloy, interconnect resistance (~100 mΩ) were developed and demonstrated on an area array test vehicle containing interconnects 5 μm in diameter on 10 μm and 25 μm pitch with a good strength of the bonded interface [17].

Another way to allow the sticking of the surface at room temperature is to provide bonding in oxide zones between the copper pads, before the metallic diffusion mechanism. This process is called the DBI™. It is a hybrid bonding; The compression,
thus diffusion, in the metal pads is induced by the temperature and the high strength of the oxide/oxide bonding part [11].

**Bonding without a compression force : direct bonding**

Direct wafer bonding refers to a process by which two mirror-polished wafers are put into contact and held together at room temperature by adhesive forces, without any additional materials [18]. This technology has become more and more attractive for microelectronic and micro technology applications because it presents many advantages, Figure 2. In this method the surfaces which may be heterogeneous or surfaces with a single type of material are bonded at room temperature. A bonder with an alignment tool capability must be used to achieve an submicron alignment [19]. Depending on the surface preparation the bonding energy can be monitored with respect to the surfaces to be bonded; as an example bonding energy of 3.8 J/m² is obtained on oxide bonding of blanket wafers with a plasma preparation with post bonding anneal [20].

![Diagram](image)

Figure 2 : Different bonding schemes used for direct bonding techniques : a) oxide bonding with precision alignment Two vias are necessary to contact the two layers b) oxide bonding with alignment the contact is achieved via capacitance [21] c) direct bonding of hybrid oxide metal patterned surface.

For copper bonding ultra high vacuum (UHV) bonding has been investigated to avoid oxide formation [22]. Prior to bonding the Cu surface are activated in a UHV plasma with an Ar ion beam to remove the copper oxide. The bonding is then done at room temperature under high vacuum, a low temperature anneal around 200°C bonding strength is enhanced [23]. Although high bonding energies (few joules per square meters) are demonstrated, the complexity of UHV tool as process through put prevents this technology from being adapted in the industry.

Direct bonding of patterned oxide/copper surfaces at room temperature and ambient air was developed by the authors. This technique will be described in details in the next section of this publication.

**Direct copper bonding mechanism**

**Room temperature**

To investigate the copper to copper direct bonding mechanism, the bonding interface at room temperature and its evolution with temperature was analyzed using complementary characterizations such as X-Ray Diffraction (XRD), X-Ray Reflectivity
(XRR) and Transmission Electron Microscopy (TEM) characterizations. 10nm TiN Chemical Vapor Deposition (CVD) and 1µm of copper (200 nm Plasma Vapor Deposition (PVD) + 800nm Electrochemical Deposition (ECD)) were deposited on oxidized 200 mm silicon wafers. Chemical Mechanical Polishing (CMP) based surface preparation was used prior to bonding ensuring a low roughness and a high hydrophilic behavior of the copper surfaces. This surface preparation was described elsewhere [24].

TEM observations in Figure 3 show a sharp interface at room temperature. At high magnification a 4 nm crystalline layer can be seen. This behavior is very different than a non metallic bonding interface. Electron Energy Loss Spectroscopy (EELS) analyses have detected the presence of oxygen in this layer. With XRR measurements on stored samples a drop of electron density of about 4 nm width was recorded. The ratio ($\rho/\rho_{Cu}$) of electron density ($\rho$) at the bond interface to the electron density of bulk copper ($\rho_{Cu}$) shown in figure 3 is in accordance with $\rho_{Cu2O}/\rho_{Cu}$, found in reference [25, 26]. This layer is thought to be the signature of the presence of a copper oxide at the interface. It can be assumed that this layer is created during the storage of the bonded wafers. XRR spectrum measured just after bonding shows a more classical shape except for the presence of a shoulder on either side of the interface which is indicative of the presence of an oxygen enriched layer.

![Figure 3: TEM images at high magnification of un-annealed copper bonded samples.](image)

The presence of a crystalline layer of 4nm width is found. XRR measurements of electron density of as bonded and stored samples show the creation of this interfacial layer with time (shown in the upper right corner box. The drop of electron density is about 4 nm width and the interface $\rho/\rho_{Cu}$ value is in accordance with $\rho_{Cu2O}/\rho_{Cu}$.

Evolution of the bonding toughness at room temperature as a function of the storage time was performed by Double Cantilever Beam (DCB) technique Figure 4. The increase of energy with storage time confirms the XRR and TEM observations. With time the bonding energy is equal to oxide bonding energy values at room temperature it increases to 1 J/m² after two days and is equal to the bulk energy value after a few months storage. The bonded pairs are sealed completely at this point with no gaps detected at the interface.
Figure 4: Room temperature bonding toughness for blanketed copper on silicon wafers as a function of storage time.

Behavior with temperature

At 200°C, the copper oxide becomes thermo dynamically unstable [27]. Its diffusion along the bonding interface is observed and diffusion bonding can happen. Nanovoids partially filled with oxide are created. A copper to copper grain boundary appears, and dislocations can be imaged at the bonding interface. XRR measurements done in temperature confirm the sealing of the interface at 230°C.

Figure 5: TEM cross section of a blanket Cu/Cu direct bonding after 200°C post bonding anneal for 30 minutes. The interfacial copper oxide diffuses along the bonding interface which allows intimate copper copper contact and creation of dislocations.

This mechanism is similar to a diffusion bonding of copper to copper except that no pressure is applied. The diffusion bonding has been extensively studied in metal sintering [28] and consists of a plastic deformation of the asperities of both metal films. In our case we have a direct bonding at room temperature of highly hydrophilic surfaces. With temperature the strengthening of the interface is obtained by a diffusion like mechanism.
Patterned copper/oxide bonding mechanism.

Due to a possible CMP non-homogeneity, the patterned surfaces might present different topologies within within a single wafer which may effect wafer to wafer bonding. It is mandatory that the bonding process is tolerant to those topologies as shown in Figure 6. This tolerance is obtained thanks to the expansion of copper with temperature that enables the bonding even if the copper is dished. In case of copper protrusions, the protrusion should be as small as possible to allow the oxide bonding.

Simulation of copper pad deformation with respect to temperature, pad size and height was done with Ansys software considering the elastic properties of silicon and silicon dioxide and elasto-plastic properties of copper. It can be seen in figure 7 that the vertical displacement of the Cu pads varies with the pad geometry. Also the results show that a small dishing of copper pad will be overcome during the post bond annealing even at low temperature such as 200°C. It is also important to point out that the monitoring of the CMP step and the knowledge of the layout needed for a good bonding is mandatory.

Very good bonding and high bonding toughness can then be obtained with respect to this bonding behavior. Acoustic observations (SAM) do not show defects bigger than 30 µm (resolution of this equipment), see Figure 8. Bonding toughness was recorded, Figure 9, it ranged from 1J/m² at 200°C up to 6,6 J/m² at 400°C confirming that the mechanism is identical to intermetallic bonding described earlier. Even after 200°C post bonding anneal it was possible to grind down to 5µm the top silicon of the bonded pair.
Copper pad diameter (µm)

Height increase at the center of the pad (µm)

Copper pad diameter (µm) 

200°C

Figure 7: Simulation of the vertical displacement of copper pads at 200°C, as a function of pad geometry. H is the height of the copper line in micron.

Figure 8: left) Acoustic image of bonded patterned wafers (hybrid oxide-metal) at room temperature, middle) same wafers after a 400°C anneal, right) Picture of a bonded pair ground down to 5 µm after a 200°C post bonding anneal.

Figure 9: Comparison of bonding toughness for bonded copper blanket ed wafers, oxide blanket ed wafers and bonded patterned oxide/metal surface wafers.
Alignment

To recover vertical interconnect in 3D technology, bonding with precision alignment is mandatory. As direct bonding is done at room temperature it maximizes throughput and eliminates contribution of wafer thermal expansion on misalignment. Therefore, the added stress to the bonded wafers impairing devices and interconnects and inducing wafer deformation are diminished or avoided. Reducing process-induced distortion is also key parameter to avoid a decrease in yield or reliability as well as to improve critical alignment accuracy.

Face to face alignment between bonded wafers was performed in a EVG tool and was measured by means of a transmission IR microscope after bonding. The misalignment was measured on a micrometric vernier in 5 locations all around the wafer (1 at center and 4 at edges: N, S, W, E). The vernier allowed an accuracy of measurement below 0.1µm. The results are given, in µm, in Figure 10.

Based on further process optimization (e.g. planarization, surface treatments, etc) alignment of less than 1 µm across the wafer has been achieved using standard alignment marks and EVG Smart View® system. For 200mm wafers, alignment below 0.2µm is shown all around the wafer. For the 300mm wafer pair, misalignment is below 1.0µm at edge. As reported in literature [29], the misalignment is a combination of an offset and a rotation between the bonded wafers and of an additional effect called run-out. The misalignment shift for both 200 and 300mm wafer pairs is below 0.2µm (respectively (0.2, 0.0) and (0.1, 0.0)). It demonstrates that the alignment control during bonding is accurate enough to ensure good alignment. As no external force or pressure is applied during wafer preparation or the direct bonding process, we obtain a minimum mechanical deformation. Thus, the wafer to wafer direct bonding process leads to excellent alignment while ensuring a very high throughput.

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Figure 10: 200m and 300mm mapping for (x, y) misalignment given in µm. A vernier with the positive and negative direction for x and y is shown top left of the figure.
Characterization of direct bonded wafers: acoustic microscopy

To study the evolution of bonded structures using SAM with temperature as the processing variable, we have used wafers with different copper line widths. To image resolution and bonding behavior with temperature, it was chosen to bond patterned wafers to blanket oxide surface with copper features in small dishing. Then these 200mm wafers were annealed successively at 100°C, 200°C, 300°C and 400°C for 2 hours.

After the wafer bonding and successive annealing, the bonding interface quality is observed using an acoustic microscope. With a 110 MHz transducer, the effective lateral resolution is 7µm and defects as thin as 5nm can be detected in the Z-direction.

In Figure 11 the evolution with temperature of a SAM signal on a set of half Kelvin crosses of sizes ranging from 15 µm to 25 µm can be seen. At room temperature, no copper areas are closed because of the residual CMP dishing: the whole features appear bright white. With temperature increase, the copper structures expand, filling the gap left by the CMP topology. When the copper surface comes into contact with the facing oxide surface, bonding occurs and SAM contrast disappears. In the smaller patterns, where the initial post CMP dishing is limited, the closing of the copper interface occurs at lower temperature (evolution is already visible at 200°C for the smallest crosses). In larger patterns, with higher dishing values, high temperature anneals are required to completely seal the bonding interface. It can be seen in Figure 11, that all copper features are completely bonded upon 400°C annealing.

Figure 11 : SAM images showing the evolution of half Kelvin cross patterns with temperature, the width of the branch is respectively from top to bottom 25, 25, 20 and 15 µm.

This experiment demonstrates that this characterization technique can be successfully used to adapt the pre and post bonding process conditions with respect to the layout.

Characterization of direct bonded wafers: electrical behavior of daisy chains

Daisy chains (DC) were used to investigate the electrical behavior of bonded structures. Different dimensions (contact area of 3x3µm² or 5x5µm²) and various numbers of connections (5000 to around 30000 connections) are tested.
The followed integration process was used to realize the electrical characterization: after bonding, the top silicon wafer is first removed down to the oxide using a combination of mechanical and chemical (TMAH) etching. The silicon oxide is finally dry etched down to bonding interface to enable probes to connect the copper pads (Figure 12).

Figure 12: Bonded wafers after the complete removal of one silicon wafer and the SiO₂ layer

Figure 14 represents an optical picture of the bonded structure after the removal of the top wafer down to the bonding interface. The measured misalignment all over the wafer is less than 1µm, and allows the connection between all the copper lines even in the highest density (3x3 µm² contact area with a pitch of 14µm on x-axis and 7µm on y-axis).

Figure 13: Optical observation of DC after the complete removal of top silicon wafer down
V(I) and R(I) characterizations for a daisy chain, with 29422 connections and a contact area of 3x3µm², after a 400 °C anneal is presented in Figure 14. A perfect ohmic behavior is observed for all the tested structures. Considering the chip size of 2 mm², the density of interconnections for this daisy chain is estimated around d=1,5 10⁶/cm².

A total chain resistance of 2.34 kΩ is measured for this daisy chain, which corresponds to a resistance of 79.5 mΩ per node (node = bonding interface + Cu lines) (Figure 15).

Comparing the experimental with the theoretical calculation of the resistance per node (that leads to a value of 77 mΩ), a difference of 2.5 mΩ is obtained [30].

\[ R_{\text{experimental}} - R_{\text{theoretical}} = 79.5 - 77 = 2.5 \text{mΩ} \]  

[1]

This difference is induced by copper line resistance variations, +/- misalignment error during bonding (impacting mainly the contact area) and the real bonding interface resistance R_c. In the worst case, where this difference is induced only by the bonding interface resistance, the estimate specific contact resistance (\( \rho_c \)) is:

\[ \rho_c = R_c \times A_c = 2.5 \times 9 \text{ mΩ.µm}^2 \sim 22.5 \text{ mΩ.µm}^2 \text{ with } A_c \text{ the contact area.} \]  

[2]

The specific contact resistance for a 400°C post bonding anneal is then around 22.5mΩ.µm². These values of resistance and specific resistance show that there is an insignificant impact of the bonding interface. And that the bonded structures have almost the same electrical behavior as copper line bulk without an interface [30].
For 200°C annealed structure, the extraction of the bonding interface resistance was achieved on daisy chain with 5x5µm² contact area. With the same assumptions as before, the bonded contact resistance is of R_c ~ 5.6 mΩ. This resistance leads to a specific contact resistance of ρ_c = 140 mΩ·µm².

The resistance obtained for the 200°C post bonding annealed sample is higher than the 400°C annealed, but this value is still very small and shows that for a 200°C post bonding anneal, there is no impact of the bonding interface on the electrical behavior.

**Matching**

In order to demonstrate the reproducibility of the electrical data at the wafer level, statistical measurements have been performed on more than 200 chips across the wafer area (200mm wafer). Figure 16 represents the distribution on more than 200 tested chips of the measured resistance of 29422 interconnected daisy chain all over the wafer (3x3µm² contact area.). The yield is 88.5%. Table 1 describes the minimum, the maximum and the average value of the global resistance of the daisy chain. It shows also a small standard deviation σ ~ 1.18% that confirms the reproducibility of the bonding process over the entire wafer.

![Figure 16: Wafer map of the 29422 daisy chain resistance](image)

**TABLE I.** Electrical measurement of 30000 interconnect daisy chains on 400°C annealed bonded wafer

<table>
<thead>
<tr>
<th>Post bonding annealing</th>
<th>Min (Ω)</th>
<th>Max (Ω)</th>
<th>Average resistance (Ω)</th>
<th>Standard deviation (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>400°C for 2h</td>
<td>2162</td>
<td>2291</td>
<td>2202</td>
<td>1.18</td>
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</tbody>
</table>

**Conclusion**

For More Moore and More than Moore applications, low temperature bonding and metal bonding are becoming the main integration paths for 3D stacking. Thermocompression and direct bonding are the main research areas being pursued. We have presented our developments on direct Cu/Cu bonding at room temperature, atmospheric pressure and ambient air. A bonding mechanism is proposed to explain copper direct bonding on blanket and patterned wafers based on interface reconstruction. Evolution of the bonding interface to a grain boundary above 200°C was presented by coupling XRD, XRR and TEM analysis. Validation of copper direct bonding electrical contact was demonstrated on 29422 interconnects daisy chains. Specific contact
resistance of 22.5 mΩ·µm was obtained for 3x3 µm² contact areas. The contact resistance of a 3x3 µm² contact resistance, 2.5 mΩ is negligible compared to the resistance of a via of 3x3 µm² which is around 130 mΩ.

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