Dielectrics in Nanosystems -and- Graphene, Ge/III-V, Nanowires and Emerging Materials for Post-CMOS Applications 3

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PREFACE

This issue of *ECS Transactions* combines the manuscripts from the “Graphene, Ge/III-V, Nanowires and Emerging Materials for Post-CMOS Applications – 3” symposium and the papers presented at the “Tutorials in Nanotechnology” symposium, with focus on ‘Dielectrics in Nanosystems.’ We hope that this combination will bring more value to our readers as a reference volume. The editors appreciate the support of all Divisions involved in its creation and the New Technology Subcommittee for enabling the tutorial chapters.

In recent years there have been four International Symposia on “Dielectrics In Nanosystems: Materials Science, Processing, Reliability and Manufacturing,” which were held during alternate ECS Spring Meetings. The latest of these meetings was Spring 2010 in Vancouver, Canada, and was co-sponsored by the DS&T Division of ECS and IEEE EDS. The topics for the tutorial materials included in this issue were selected based on the four previous symposia and the current direction of research that novel dielectrics play in nanosystems.

After two successful symposia in Vancouver (2010) and San Francisco (2009), the “Third International Symposium on Graphene, Ge/III-V, Nanowires and Emerging Materials for Post-CMOS Applications,” held in Montreal from May 2-4, 2011, which brought together an excellent set of papers from different parts of the globe emphasizing “More-Than-Moore” systems and continue to bridge the gap between advanced CMOS and “Post-CMOS systems”. In the quest of achieving high speed and high mobility low power devices, Ge for PMOS and III-V for NMOS are more near-term exploratory materials, whereas, Nanowires and Graphene are next generation materials following Ge/III-V technology nodes. In addition, due to its better thermal and transport properties, Graphene is uniquely positioned to support “Post-CMOS” era applications.

In the first chapter of this issue, there are five tutorials presented by world leaders on “Dielectric in Nanosystems”. The perspective of nanotechnology and its convergence with future information technology is discussed in the first one. The second one provides a status review of nanocrystals embedded high-k nonvolatile memories. The third one brings the silicon nanowire field effect transistor technology. The fourth one addresses the physics of nanonet fabrics and its applications in electronic, optical, biosensing, energy storage, and MEMS devices and systems. The fifth one brings the next generation sensor systems for healthcare and homeland Security.

In the second part of this issue, “Graphene, Ge/III-V, Nanowires and Emerging Materials for Post CMOS Applications – 3,” the papers represent many of the leading research groups in the field. The symposium started with four plenary papers given by leading groups on Ge-source TFETs, Graphene Nanoelectronics, III-V Channels, and Nanowire Electronics respectively. The first speaker, Prof. Tsu-Jae King Liu of University of California, Berkeley also won “2011 Thomas D. Callinan Award” sponsored by Dielectric and Science Division. Rearranging some of these papers, the
second chapter of this issue contains the papers presented on “Nanowires and Exploratory Materials for Post CMOS Devices.”

In the Graphene related section, a total of 15 papers were presented covering the following areas: 1) Graphene Material Preparation, Synthesis and Characterization; 2) Graphene Field Effect Transistors and Electronics, and 3) CNT Field Effect Transistors and Electronics. These papers are represented in the following two chapters (Chapter 3 and 4).

In the Ge/III-V related section, a total of 23 papers were presented covering the following areas, published in subsequent five chapters: 1) III-V High Mobility Channel FETs : Fabrication and Characterization, 2) III-V High Mobility Channel FETs : Device Optimization, 3) Gate Dielectric and III-V MOSFET : Interface and Performance, 4) Ge and SiGe High Mobility FETs : Fabrication and Characterization, and 5) Ge Based Devices : Device Optimization for Gate Dielectrics and Contacts. Here, we have drawn extensively on the university and industry groups affiliated with SRC-NRI programs in Beyond CMOS. For this, we wish to acknowledge the SRC-NRI program’s tacit support for these symposia.

We would like to express our sincere appreciation to the tutorial presenters and all the authors who contributed to this issue of ECS Transactions. Their dedicated effort in preparing and submitting the manuscripts is highly appreciated. They have allowed us to hopefully produce a more valuable volume to our readers within short time.

We are also grateful to the staff of The Electrochemical Society, particularly Paul Urso, John Lewis, and Beth Anne Stuebe, who helped us at various stages, preceding, during, and after the symposium, and during the publication period. Finally, the success of the symposium would not have been possible without the financial support given by Dielectric Science and Technology Division, and the New Technology Subcommittee as well as the continuous sponsorship provided by AIXTRON for the last three years.

We hope that this combined issue will bring more value to our readers who are interested and focused on Dielectric Nanosystems and low power high speed nano-electronics based on Graphene, Nanowires and Ge/III-V materials.

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May 2011
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