Cleaning Challenges and Solutions for Advanced Technology Nodes

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Trends in further scaled CMOS technologies are reviewed with respect to the implications for cleaning and wet processing. Particularly the FEOL processes are being considered such as selective cap removal, pre-epi cleaning and post I/I photo resist removal. For technologies beyond the 15nm, several aspects of wet processing of potential new materials, such as Ge and III-V, and advanced integration schemes are covered.

Geneal Aspects of Gate First and Replacement Gate Processes

Different Approaches for VT Control

In the gate first scheme obtaining appropriate threshold voltage ($V_T$) for the High Performance (HP) p- and n-MOS transistor is very challenging. A single metal gate (e.g. TiN) using dual cap-layer has been introduced. For the n-MOS such cap layer can consist of 3nm La$_2$O$_3$ or a few nm of MgO. For the p-MOS it can be a few nm of Al$_2$O$_3$. The cap layers are coated with BARC and photo resist (PR) for one polarity of transistors in order to selectively remove the cap layer for the other polarity. After this cap removal patterning the photo-resist and BARC need to be removed with very high selectivity towards the cap layer material. SPM (90C) cannot be used as it etches Al$_2$O$_3$ at approx 4nm/min and La$_2$O$_3$ at a rate in excess of 100nm/min. La$_2$O$_3$ and MgO are very sensitive to aqueous solutions in general. Therefore instead of using SPM, solvent-based PR and BARC removal is proposed. Fig.1 shows the time to remove the PR and BARC as well as the etch rates for Al$_2$O$_3$ and La$_2$O$_3$.

As an example the performance of Dimethyl sulfoxide (DMSO) with small amounts of TetraMethylAmmonium Hydroxide (TMAH) added have been evaluated using an N2 based aerosol spray dispense (DNS SU3000) \cite{1}. In the case of La$_2$O$_3$ exposed, only mixtures with a TMAH content of at least DMSO:TMAH=100:1 provide a large process latitude. A solution with a volume mixing ratio in the range of DMSO:TMAH=100:1 to 500:1 provides acceptable process margin for both La$_2$O$_3$ and Al$_2$O$_3$.

In case after PR strip a water soluble film such as La$_2$O$_3$ or MgO cap is exposed also the post PR-strip rinsing solution needs to be optimized. It was shown that isopropanol (IPA) rinsing could reduce the loss of MgO to less than 0.1 nm/min.
Figure 1. Etch rate of Al$_2$O$_3$ and La$_2$O$_3$ and time to completely remove the photo resist and BARC in an liquid aerosol spray made from a heated mixture of DMSO and TMAH as a function of the volume mixing ratio [1].

The solvent based PRstrip tends to leave residual particles behind and requires a post-strip particle removal step. These particles are effectively removed in NH$_4$OH or in APMixtures. This can be applied for La$_2$O$_3$ but not for Al$_2$O$_3$. In case TiN is exposed dilute NH$_4$OH should be used in absence of H$_2$O$_2$. If Al$_2$O$_3$ is exposed a plasma based process has been found to efficiently remove the residue, without any risk of Al$_2$O$_3$ loss.

With further down scaling of the equivalent-oxide-thickness (EOT) the Vt of the HP p-MOS is decreasing (i.e. negative values with increasing absolute value) to the extent it cannot meet the target for the 22 nm node. Appropriate channel engineering for the p-MOS has proven to be the appropriate solution. The use of SiGe channel layers for the p-MOS with a Ge content of 45 to 55% are found to result in an appropriate VT, even in the absence of an (Al$_2$O$_3$) cap layer. In addition it provides a current boost due to the increase in hole mobility. The SiGe channels are typically grown early on in the process flow (see Fig. 2).

Figure 2. The growth of SiGe channel for the p-MOS requires clean and oxygen free surfaces, prior to the epi growth.
The pre-epi surface needs to be very clean. In this stage in-situ bake can still be done at relatively high temperature as there are no severe thermal budget limitations. Therefore this pre-epi clean is somewhat less critical than others further down-stream in the process. Dual metal replacement gate schemes both with high-k first or high-k last can also meet the Vt targets, at the expense of significant process complexity.

Post-Lightly Doped Drain Ion Implanted Photo Resist Removal

After the gate stack has been patterned halo and extension ion implantation is applied. Multi I/I implantations are done to specific parts of the chip while other areas are protected by a photo-resist layer. In typical process flow several such post Lightly Doped Drain (LDD) I/I photo resist strips have to be performed. Because of finite selectivity each strip may result in a (limited) attack of the exposed materials as is depicted in Fig. 3 for the case of a gate first approach. The strips of the most shallow I/I are performed as last steps in order to minimize the loss of doped semiconductor material. The gate stack overetch and preceeding strips can lead to loss of undoped semiconductor and could create a recess, expected to be less critical than the loss of doped semiconductor. In general one can expect that a loss of 2 to 3 nm could be tolerated. In case of (Si)Ge channel material one has to carefully control the strip process, as such materials are very sensitive to chemical attack. In case of thin “substrates” such as in planar SOI or in finFETs, however, this undoped semiconductor loss is much more critical. Losing doped semiconductor material leads to an increase in series resistance and thus to a reduction in drive current. In order to limit the dopant loss to less than 20% the total loss of doped substrate during all the strips and cleans should be kept typically below 0.8 nm for planar devices and below 0.3 nm for finFETs (with 7° tilt implants). It is important to consider the total loss of the entire process as one specification. Indeed the first strip process may results in the formation of an oxide which result in a significant loss of doped semiconductor. But if subsequent treatment do not significantly attack this oxide the overall a process will be acceptable. Besides the loss of semiconductor substrate material also the lateral loss of the metal gate electrode should be limited (e.g. < 1 nm) in order to maintain gate control up to the edges of the channel. The lateral loss of high-k gate dielectric should be less than the loss of the metal in order to avoid dielectric failure.

Figure 1. Critical material loss aspects to gate stack LDD PR strips and cleans. The right side of the transistor shows the critical issues in terms of material loss due to the multiple LDD I/I and PR strip and clean processes, here shown for a gate first approach. The left side show the final gate stack. (The halo implant is not shown to simplify the picture.)
Typically sulfuric acid based oxidizing mixtures have been applied for such photo resist strip processes. This approach, however, is not compatible with SiGe (Ge > 50%). For gate first processes also it is not compatible with some of the gate dielectric materials and particularly with cap layers and the metal gate materials, as can be seen from Table I.

Table I. Etch rates of different gate stack materials by SPM.

<table>
<thead>
<tr>
<th>Material</th>
<th>Clean</th>
<th>Etch rate (nm/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TIN</td>
<td>1/4 SPM at 90 C</td>
<td>19 ± 2</td>
</tr>
<tr>
<td>Ta2C</td>
<td>1/4 SPM at 90 C</td>
<td>0.06 ± 0.01</td>
</tr>
<tr>
<td>HfO</td>
<td>1/4 SPM at 90 C</td>
<td>~0</td>
</tr>
<tr>
<td>HfSiON</td>
<td>1/4 SPM at 90 C</td>
<td>~0</td>
</tr>
<tr>
<td>AlO</td>
<td>1/4 SPM at 90 C</td>
<td>4.3 ± 0.14</td>
</tr>
<tr>
<td>DyO</td>
<td>1/4 SPM at 90 C</td>
<td>8.25</td>
</tr>
<tr>
<td>LaO</td>
<td>1/4 SPM at 90 C</td>
<td>&gt;144</td>
</tr>
<tr>
<td>sSiGe 20%</td>
<td>1/4 SPM at 90 C</td>
<td>~0.002</td>
</tr>
<tr>
<td>Ge</td>
<td>1/4 SPM at RT</td>
<td>~140</td>
</tr>
<tr>
<td>GaAs</td>
<td>1/4 SPM at RT</td>
<td>~400</td>
</tr>
</tbody>
</table>

Therefore solvent based solutions are currently being considered. Fig. 4 shows that mixtures of NMP and AEE were found to be compatible with a wide range of gate stack materials.

Figure 4. The etching of a wider range of gate stack materials can be kept very low in case of a solvent mixture of NMP/AEE (1/1) at 80C (left table). For AlO the etching virtually vanishes once the NMP/AEE ratio exceeds 3000/1, as shown in the right graph.

Source Drain Formation

In conventional processes after spacer formation source and drain are obtained by high-dose (HD) I/I for each polarity of the transistor separately while the other polarity being shielded by photo resist. Removing the HD implanted photo-resist occurs in some cases with very aggressive sulfuric acid based oxidizing solutions. Such processes may lead to attack of the Si3N4 spacers (possibly by similar mechanisms as attack by high temperature and high pressure water [2]). State-of-the art is to selectively grow in-situ doped source and drain in an epi reactor. The growth of SiGe SD for the p-MOS is widely used to introduce strain and hole mobility increase. For FinFETs such selective deposition of source and drain is even more important to locally increase the thickness of the fin and thus reduce the series resistance. The surface preparation prior to the epi-step
is very critical as the presence of shallow extension junction prohibits long time high
temperature in-situ pre-bake to remove contaminants and chemical oxide layers.
Watermark-free HF surface preparation and drying is required.

Gate-Last Processes

Gate last processing requires appropriate removal of the dummy silicon gate using
e.g. TMAH at high temperature. More details on this process are provided in Ref. [3].
After removal of the dummy Si, in the case of a dummy dielectric process, also this
dummy gate dielectric needs to be removed selectively. Possible critical aspects and
issues are described in Ref. [4].

Beyond 15 nm Node

For technology nodes beyond 15nm, scaling down using the current semiconductor
materials will not provide sufficient performance improvement. The use of high-mobility
channels would solve this issue. The mobility increase using strained Si for the p-MOS
was already a first step in this direction. With the use of other semiconductor materials
this mobility can increase even more. Therefore Ge is considered for the p-MOS channel
and III-V materials for the n-MOS. The use of high-k gate dielectric materials, instead of
thermally grown SiON, has lowered the technological barrier for a transition from silicon
to other semiconductor materials.
To be economically viable for mainstream CMOS applications the Ge and III-V materials
will have to be integrated on a large Si wafer. Different approaches are being explored.
For Ge blanket GOI (Germanium-on-Insulator) and GOS (Germanium on Silicon)
techniques are evaluated as well as local epitaxial growth. III-V materials are typically
depositied with local epitaxial growth as well. Because of the large lattice mismatch
buffer layers are used to reduce the defect density in the active layers.
Instead of inversion mode transistors, quantum well (QW) devices are proposed (see Fig.
5). In this structure a narrow bandgap material is sandwiched between a wide bandgap
“substrate” and a very thin wide bandgap top layer. The gate dielectric and electrode are
stacked on top of this thin layer. The current channel of the transistor is the narrow
bandgap layer. The source and drain are made implant-free (IF) by growing selective
doped epi. These QW devices show good electrostatic control of the channel and reduced
short channel effects. For the p-channel Ge could be grown on SiGe while the n-channel
could be InGaAs grown on InP.

Figure 5. Co-integration of high mobility implant-free quantum well devices for high
performance CMOS core with conventional Si CMOS for less critical circuits, all on a Si
substrate.
Post-CMP and Pre-Epi Cleaning of SiGe and III-V Buffer Layer

As mentioned above the new high-mobility channel materials can be integrated on silicon carrier wafers inside narrow trenches using selective epitaxial growth [5] as schematically depicted in Figure 6.

![Figure 6. Schematic representation of process flow for fabrication of thin high-mobility QW channel layers on Si carrier wafers using local deposition techniques.](image)

Narrow trenches in SiO₂ on silicon wafers are made using Shallow Trench Isolation (STI) patterning technologies. In these trenches, high quality crystalline epitaxial layers are selectively grown (a). After chemical mechanical polishing and controlled etch back of the buffer material (b), this substrate serves as the starting template for fabrication of high mobility QW channel layers by epitaxial growth (c). After deposition of the channel, the gate stack with the gate dielectric and electrode can be constructed and the transistors can be processed.

After the CMP and prior to channel deposition, the presence of a clean and well-ordered surface on an atomic level is necessary. Therefore a wet cleaning step with well-controlled and limited substrate attack is indispensable to remove all the contaminants. Different parameters need to be investigated, such as overall etch rates and preferential attack of individual components of the compound semiconductors.

SiGe Compatibility.

No significant etching of SiGe and Ge (< 0.2 nm/min) is observed in non-oxidizing HCl/HF aqueous solutions. In acids, such as HNO₃ and H₂SO₄, Ge shows a low etch rate on the order of 0.15 nm/min. All of these non-oxidizing acid cleans can be considered to be compatible with SiGe and Ge.

In aqueous oxidizing environments such as ozonated DIW (O₃-DIW, see Table II), however, significant etching of Ge occurs. For concentrated NH₄OH/H₂O₂/H₂O (APM) mixtures at room temperature the etch rate of Ge get almost as high as 1 µm/min (see Figure 7)! These high etch rates are attributed to the high solubility of GeO₂ in aqueous solutions. Upon dilution of the APM mixtures, a moderate decrease in the etch rate can be observed. Figure 7 also shows that, the etching of SiGe strongly decreases with decreasing germanium concentration. In addition, it has been reported that in case of exposure of SiGe to an APM (1/4/20) mixture a thick Si-rich oxide layer is growing [6]. These layers are most likely porous. The formation is attributed to the selective dissolution of the GeO₂ that is formed, leaving behind the SiOₓ. The exposure of SiGe to APM should therefore be restricted to short times and very dilute composition such as 1/1/5000.
Table II. Etch rates of SiGe (ellipsometry) and Ge (weight loss) (nm/min) in different mixtures at RT [7].

<table>
<thead>
<tr>
<th></th>
<th>Si$<em>{0.45}$Ge$</em>{0.55}$</th>
<th>Si$<em>{0.55}$Ge$</em>{0.45}$</th>
<th>Ge</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>HCl:H$_2$O (1:8)</td>
<td>&lt;0.017</td>
<td>&lt;0.05</td>
<td>&lt;0.04</td>
<td>[5]</td>
</tr>
<tr>
<td>HF:HCl:H$_2$O (1:10:70)</td>
<td>&lt;0.086</td>
<td>&lt;0.16</td>
<td>&lt;0.08</td>
<td>[5]</td>
</tr>
<tr>
<td>2 w-% HF</td>
<td>&lt;0.090</td>
<td>&lt;0.099</td>
<td>&lt;0.11</td>
<td>[5]</td>
</tr>
<tr>
<td>1 M HNO$_3$</td>
<td>-</td>
<td>-</td>
<td>0.14±0.013</td>
<td>[6]</td>
</tr>
<tr>
<td>96 w-% H$_2$SO$_4$</td>
<td>-</td>
<td>-</td>
<td>0.16±0.006</td>
<td>[6]</td>
</tr>
<tr>
<td>H$_2$O</td>
<td>&lt;0.022</td>
<td>&lt;0.049</td>
<td>&lt;0.036</td>
<td>[5]</td>
</tr>
<tr>
<td>H$_2$O (O$_2$-bubbling)</td>
<td>-</td>
<td>-</td>
<td>0.005</td>
<td>[6]</td>
</tr>
<tr>
<td>DIW-O$_3$ (1 w-ppm)</td>
<td>0.15±0.23</td>
<td>0.24±0.28</td>
<td>1.1±0.1</td>
<td>[5]</td>
</tr>
<tr>
<td>pH 11 NH$_4$OH (1:100)</td>
<td>-</td>
<td>-</td>
<td>0.29±0.007</td>
<td>[6]</td>
</tr>
</tbody>
</table>

*: not measured

Figure 7. Etch rates of Ge (weight loss), SiGe and InP (ellipsometry) in APM at RT as a function of volume mixing dilution ratio.

In order to evaluate different cleaning processes on their capability of removing surface oxides, Si$_{0.45}$Ge$_{0.55}$ layers where oxidized in a dry UV O$_3$ furnace at room temperature. Concentrated HCl does not noticeably remove any of the oxides. Diluted NH$_4$OH (1/100) was found to effectively remove SiO$_x$ and to some degree also GeO$_x$. HF was found to be most effective in removing both types of oxides. After the HF exposure of SiGe, Ge-H stretch peaks were observed in ATR-FTIR.

InP Compatibility.

In Table II, an overview is given of the etch rates of InP in typical cleaning mixtures. It is shown that InP is etched in acidified solutions. Especially in concentrated HCl, a high etch rate is observed. However there is a risk for the production of the toxic gas PH$_3$ in HCl containing solutions [8, 9]. Table II also shows that, at low pH, the dissolution rate of InP is further increased if an oxidizer such as O$_3$ is present. At neutral pH with an oxidizer, such as DIW-O$_3$ mixtures, the etching is limited. Also in alkaline solutions, such as diluted NH$_4$OH, the InP is not etched unless an oxidizer is added. Figure 7 includes the etch rates of InP in APM mixtures at different dilutions and as shown in this graph, only for the most concentrated 1:1:5 mixture, a significant etching is
observed. Similarly to SiGe, there is a risk for InP to alter the surface composition by using oxidizing chemistries due to the differences in solubility of the oxides.

Table III. Etch rates of InP (nm/min) in different cleaning chemistries [7].

<table>
<thead>
<tr>
<th>Etch rate (nm/min)</th>
<th>InP</th>
</tr>
</thead>
<tbody>
<tr>
<td>37 w-% HCl</td>
<td>10 ± 349</td>
</tr>
<tr>
<td>3.7 w-% HCl (1:10)</td>
<td>2.5 ± 0.2</td>
</tr>
<tr>
<td>0.37 w-% HCl (1:100)</td>
<td>&lt; 0.05</td>
</tr>
<tr>
<td>0.037 w-% HCl (1:1000)</td>
<td>&lt; 0.05</td>
</tr>
<tr>
<td>2 w-% HF</td>
<td>&lt; 0.2</td>
</tr>
<tr>
<td>0.5 w-% HF</td>
<td>&lt; 0.19</td>
</tr>
<tr>
<td>0.05M HF/3.7% HCl</td>
<td>0.07 ± 0.01</td>
</tr>
<tr>
<td>69 w-% HNO₃</td>
<td>0.68 ± 0.09</td>
</tr>
<tr>
<td>96 w-% H₂SO₄</td>
<td>5.56 ± 0.31</td>
</tr>
<tr>
<td>1M NH₄OH</td>
<td>&lt; 0.21</td>
</tr>
<tr>
<td>DIW-O₃</td>
<td>&lt; 0.4</td>
</tr>
<tr>
<td>0.037 w-% HCl + O₃</td>
<td>0.75 ± 0.41</td>
</tr>
<tr>
<td>1:1:5 APM</td>
<td>1.01 ± 0.2</td>
</tr>
<tr>
<td>1:1:50 APM</td>
<td>&lt; 0.19</td>
</tr>
<tr>
<td>1:1:500 APM</td>
<td>&lt; 0.19</td>
</tr>
</tbody>
</table>

On the InP the following oxides have been identified on the surface by XPS: InPO₄, InPO₃ and In₂O₃. The removal of these residual oxides from the surface is still under investigation. Possible candidate mixtures are dilute HCl, dilute H₂SO₄, dilute HF or NH₄OH. Low pH mixtures seem to be efficient, yet oxide free surfaces have not yet been observed. On a dilute H₂SO₄ treated InP surface the oxides were found to grow relatively rapidly during exposure to the clean room air.

Particle Removal.

The removal of slurry particle from Ge was investigated. Different chemistries were evaluated. It was found that good particle removal was obtained if 3 nm of material was removed (similar to Si) (Fig. 8).

![Figure 8](image-url)
Pre-ALD Surface Preparation of SiGe and III-V Materials

Finding a high quality gate dielectric that can lead to a well passivated interface with sufficiently low density of interface states remains a major challenge for both Ge and III-V compound semiconductors.

For Ge, wet aqueous cleaning solutions can easily remove GeO₂ but it is rather difficult to completely remove GeO (or suboxides) [10]. For GaAs it is difficult to completely remove oxides by wet cleaning. HCl removes some of the native oxide.

The initial growth of ALD of HfO₂ has been studied on differently prepared surfaces [11] and compared to an ideal 2-dimensional (2D) growth model. The presence of voids can be detected by measuring the substrate signal as a function of the total amount of Hf deposited. For both Ge as well as for GaAs substrates initially the growth did not have a 2D character. As deposition proceeds a turning point is reached where layer closure is obtained and the growth proceeds in a 2D mode. For both Ge and GaAs the treatment that is expected to leave most oxide on the surface resulted in earlier closure of the growing HfO₂ film. The substrate signal decreases as dielectric film growth proceeds until a background level is reached.

![Graph showing substrate signal vs. total Hf deposited](image)

**Figure 9.** The substrate signal (measure for presence of voids in the growing film) as a function of the total amount of Hf deposited as ALD deposition proceeds. Two types of growth regimes can be distinguished [11]

Theoretical calculations have shown that the Ge–GeO₂ interface is of high quality and has low density of states [12]. Very high mobility has been demonstrated but the mobility very strongly decreases with decreasing EOT. Moreover GeO₂ reacts with water and has limited thermal stability. In-situ grown GeO₂ in combination with La-Al-oxide dielectric layers have been shown to result in good surface properties.

Still the presence of thin GeO₂ layers makes the structure very vulnerable to undercutting of the liner/spacer by aqueous cleans (e.g. post-spacer clean) or in case of a replacement...
gate, during dummy dielectric removal etch. In such case S/D selective epi will grow underneath the spacer leading to unacceptable gate to SD leakage.

Pre-ALD Ge surface functionalisation with sulfur has been considered as well [13]. Immersion in an aqueous \((\text{NH}_4)_2\text{S}\) solution leads to S-coverage that saturates at the level of 1 monolayer. Little oxygen is measured on the surface. Encouraging p-channel mobility has been obtained for 7nm \(\text{Al}_2\text{O}_3\) dielectric and 2nm \(\text{Al}_2\text{O}_3 + 2\text{nm HfO}_2\) dielectric.

Particularly successful has been the use of a very thin (a few to 5 monolayers) of Si capping layer grown on top of Ge. This approach makes use of the excellent electronic properties of a Si/ SiO\(_2\) interface. It results in high channel mobility for the p-MOS as the valence band offset keeps the holes forming the channel in the Ge. Using this approach in combination with HfO\(_2\) dielectric EOT has been scaled to 0.85nm. The approach does not work for the n-MOS as the band-offset at the conduction band is too small and thus more a Si-like channel would be obtained. For GaAs and InGaAs sulfur passivation combined with ALD high-k dielectric layers has been shown to improve the interface properties.

Conclusions

FEOL wet processes for advanced technology nodes have been reviewed. Solvent based photo resist strip has been developed for selective cap removal. The material loss involved in removal of I/I photo resist has been explained and solvent based solutions have been proposed. Technology nodes beyond 15nm most likely will use high mobility substrates. The high mobility substrates will be deposited in small areas on Si wafers. Implant-free quantum well devices under consideration will use less post I/I photo resist strips. In contrast, more critical post-CMP and pre-epi cleaning will be required. The use of different cleaning mixtures for SiGe and InP have been explained. Finally different methods of pre-ALD surface preparation on the high mobility substrates have been discussed.

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