Embedding Device Solutions in Engineered Substrates

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A review of the advances in Smart Cut engineered substrates and the impact on device architecture and IC design is given. Primarily focusing on CMOS applications, mobility enhancing substrates, fully depleted device compatibility to SOI product capability and multi-gate FinFETs will be reviewed.

Introduction

A simple structure like silicon on insulator (SOI) has allowed the IC industry to optimize the MOSFET architecture by reducing parasitic capacitances to the substrate, cutting device leakage, improving device speed while reducing power consumption, decreasing considerably soft error rate, and so forth. The benefits and potential of SOI have been known since the 60’s [1]. The real issue for an industrial SOI development was SOI substrate availability and wafer quality. This roadblock vanished with the invention of Smart Cut™ [2, 3], a single crystal thin layer transfer technology. The simplicity of this technique underlines simultaneously the power and potential of Smart Cut technology and explains why it has become today the industrial standard for thin layer transfer [4].

Smart Cut technology consists in defining a splitting region within the donor substrate by ion implantation (e.g. H), which allows a thin film to transfer to a handle wafer after bonding and splitting. The thickness removed from the donor wafer is negligible compared to the total wafer thickness. Consequently, the donor wafer can be reused many times. A range of 10 nm up to a few 10³ nm in top Si and buried oxide (BOX) thickness is easily covered by this technology.

Beyond SOI, Smart Cut technology opens the door to substrate engineering, i.e. the capability to design new substrates tailored to specific applications [5]. It is possible to amplify certain device properties while weakening others by combining different materials or crystal orientations, adding strained layers, or simply creating a new composite substrate.

High performance ICs continue to be the driver for a specialized family of advanced substrates. Ultra-thin (UT) SOI, mobility enhancing substrates like strained SOI (sSOI) in addition to local strain techniques [6], as well as improved thermal dissipation to reduce the impact of hot spots on MOSFET performance are among the most obvious engineered substrate solutions [5]. Direct silicon Bonding (DSB) adds a high-end mobility enhancing substrate to the bulk Si IC architectures [7]. Non-planar device architectures like FinFETs take advantage of the buried oxide or nitride as an etch stop for fin height definition, thus reducing fin variability [5].

A review of the advances in Smart Cut engineered substrates and the impact on device performance and IC design is given below.
High Performance Substrates

Beyond the 90nm technology node, the electron and hole mobility enhancement have become essential to assure device performance increase while scaling. Two approaches are clearly identified: strained silicon, and dual crystal orientation surfaces. The first one is evolutionary and takes advantage of strain inducing CMOS processes which can be further amplified by combining them with a strained silicon substrate (sSOI) [8,9]. The alternative and probably complementary approach is the dual crystal orientation surface with (100) and (110) Si surfaces for the n and p-channels, respectively [7, 10]. Beyond 32nm, a hybrid material surface with tensile Si and compressive Ge or SiGe for the n and p-channels, respectively, may be the path to further mobility increase [11, 12].

Strained Silicon on Insulator

Mobility enhancement has become a standard scaling parameter to assure a device performance increase for sub-90nm device geometries. Different types of stressors are used to induce the appropriate strain in the n and p channel regions. Probably the most effective stressors are the embedded SiGe (eSiGe) in the p+ source and drain regions which induce a strong compressive stress [13], and the contact etch stop layers (ESL) encapsulating the gate which can induce a tensile or compressive stress depending on the nature of the film [14]. Stressors are most effective for the smallest geometries but, paradoxically, their process window is limited by gate and active area pitch. As schematically shown in figure 1, decreasing the gate-to-gate spacing limits the effective ESL thickness.

Figure 1. Schematic representation of the gate pitch imposed limitation on ESL thickness. The gap filling limits the ESL efficiency in transferring the stress into the channel.

Transistor layout and final printed features and the gate to S/D misalignment also affect strongly the resulting channel stress for deep sub-µm geometries. Figure 2 shows the impact of gate pitch on the efficiency of ESL stressors in the range of –650 MPa to –450 MPa for compressive ESL, and in the range of 350MPa to 400MPa for tensile ESL. The way to overcome these limitations is to build the devices on a uniformly strained Si surface that is transferred onto a Si substrate with a buried oxide in between to stabilize the strained Si film and isolate it from the substrate. The resulting substrate is strained silicon on insulator (sSOI). The wafer level strain is generated by epitaxial techniques. The principle for sSOI fabrication is to generate a relaxed Si$_{1-x}$Ge$_x$ epitaxial template on a Si substrate followed by a Si epitaxial step [6]. The epitaxial Si will retain the in-plane lattice constant of the template, resulting in a biaxial strained Si film if the thickness is below a certain critical value. Typical built-in stress is around 1.3GPa. sSOI has been developed as the solution that offers higher carrier mobility, combining the advantages of SOI with those of strained silicon [6]. The fundamental difference between the uniaxial...
stressors and the wafer level (baxial) strained Si is that the former is introduced during CMOS processing while the latter is built into the substrate. As a consequence, sSOI wafers offer tensile strain for large geometry devices like in ESD and I/Os circuits, giving IC design a further degree of freedom.

Figure 2. Impact of gate poly pitch on gate encapsulating contact etch stop layers (ESL) stressor efficiency in terms of current drive IDsat enhancement. cESL stands for compressive strain inducing ESL and dESL for dual compressive/tensile ESL. Courtesy of B.Y. Nguyen, Freescale.

On-going work by IC makers and research institutes [9, 12, 15] show that the combination of uniaxial stressors and sSOI amplifies the mobility enhancement of both n- and p-channel devices. Published data [15] for Lg=35nm show that sSOI combined to tensile ESL results in an on-current (IDsat) enhancement of 18% over tensile-ESL optimized n-channel transistors, which is equivalent to an overall IDsat boost of 27% over standard SOI n-channel devices. The mobility enhancement is very significant, almost 40%. In the long channel regime mobility enhancement is about 80%.

Figure 3. A significant p-channel IDsat increase is obtained for both compressive ESL and eSiGe in combination with sSOI substrates. From A. Thean et al. [15].

For a fully depleted architecture with metal gate and high k dielectric the IDsat increase through sSOI is of 16% at Lg=25nm. For the p-channels a uniaxial relaxation of the sSOI strain is induced by selective amorphization coupled to the active area layout [15]. As a result the p-channel strain can be engineered very effectively with a compressive component along the channel and while keeping the tensile component across the channel. A 23% IDsat enhancement is obtained over unstrained SOI p-
channels. Figure 3 and 4 show the results obtained for p- and n-channel devices on sSOI in combination with ESL and eSiGe stressors, respectively.

The scalability of sSOI has been thoroughly investigated for ultrathin body sSOI with the fabrication of short $L_g=25\text{nm}$ and narrow channel $W_g=25\text{nm}$ devices [16], as well as the benefits of 40 to 50nm thick super critical strained SOI (SC- sSOI), for partially depleted (PD) MOSFETs [15], and FinFET structures [17]. Recent results also show that 2.5GPa strained Si sSOI can be manufactured [18] opening further the process window for sSOI based stressors.

![Figure 4. Almost an additional 20% current drive increase can be obtained by combining tensile ESL with sSOI substrates. From A. Thean et al. [15].](image)

**Dual Crystal Orientation Surface**

The fabrication of hybrid orientation substrates has led to the development of CMOS technologies in which n-channel transistors are fabricated on a (100) Si surface and p-channels on a (110) Si surface. The driver for this approach is the fact that the hole mobility doubles for the (110) surface along the $<110>$ direction as compared to the widely used (100) surface. Hybrid orientation composite SOI (HOT) is fabricated by transferring a (110) Si layer onto a (100) handle wafer. A (100) film on a (110) is another variation of a hybrid substrate [19]. For 40nm long pMOSFETs fabricated on a (110) surface, a current drive increase of 45% is achieved, but in contrast, the n-MOSFET on the (110) plane is degraded by 35% [19, 20]. To overcome the n-channel degradation, windows corresponding to the n channel regions are etched in the substrate through the buried oxide down to the (100) handle substrate. Then Si selective epitaxial growth follows after a spacer formation. A strong overgrowth is required to drive defects out of the active area with facet formation above the substrate plane. A final CMP steps planarizes the topography and a composite wafer with (110) and (100) regions embedded in the same surface is obtained [19]. The obvious drawback of this approach is that one of the devices is fabricated on bulk. It is a mixed bulk-SOI CMOS design.

An alternative approach proposed recently [21] for making wafers by Direct Silicon Bonding Si (DSB) is based on the idea that it is possible to change the orientation of selected Si regions by an amorphization templated recrystallization process. Here the selected top regions are amorphized by ion implant, and solid phase epitaxial (SPE) regrowth is initiated from bulk Si of the desired orientation as shown in figure 5. This new approach is fully compatible with conventional bulk CMOS technology and 35% improvement in PMOS performance has been demonstrated [7]. The DSB wafers with
top (110) Si seem to provide more straightforward CMOS integration because the SPE of (100) Si results in fewer crystal defects than that for (110) Si.

Figure 5. DSB cross section of a DSB substrate with STI separating the p-channel region on a (110) surface on the left hand side and the SPE converted (100) region on the right hand side. From C.Y. Sung et al. [7].

The DSB substrate fabrication represents a major challenge. The Smart Cut conditions have to be re-developed to take into account the absence of buried oxide and in particular the bonding becomes critical [22]. The contact between the top and substrate Si must be ohmic, oxide precipitates at the bonding interface must be minimized during Smart Cut processing and residual SiO₂ eventually dissolved in a high temperature anneal. Bonding two different crystal orientations introduces a two-dimensional dislocation network as a result of the misorientation of (100) and (110) surfaces. Results at present are very encouraging as shown in figure 6, although further work is required to improve the crystal quality of DSB as well as the interaction of these substrates with the subsequent CMOS processing and specially the SPE regrowth.

Figure 6. TEM of the DSB wafer and a HRTEM image of the bonding interface. The interface is atomically closed with no SiO₂ precipitates and no threading dislocations generating at the interface. From K. Bourdelle et al. [22].

**Fully Depleted Substrates**

**Ultra thin SOI**

Full depletion happens when the depletion region covers the whole transistor body. The coupling between gate bias and inversion channel results in improved subthreshold characteristics and weaker short channel effects as compared to Si bulk or partially
depleted device architecture. The drawback is that the FD device design is very sensitive to Si channel thickness variations. Thickness variations translate into threshold voltage $V_T$ changes. This has been the reason for the strong domination of the partially depleted architecture. With the coming of age of Smart Cut SOI manufacturing, thickness control for both the buried oxide and the top Si have ceased to be an issue for FD devices. The top Si layer total thickness variation (LTTV) is within ±1nm for all wafers and all sites [23]. This is obtained through wafer-to-wafer control on both the mean silicon and buried oxide thickness within 0.5nm. The within wafer range (max – min) and the wafer to wafer range are shown in figure 7. Similar layer thickness control is obtained for Si films down to 200Å.

![500/1450 XUT +/- 10 Å - SOI Thickness distribution](image)

Figure 7. Thin SOI product capability: pattern of 41 points/wafer, 3 mm edge exclusion. The statistic shown corresponds to 1500 Wafers. From C. Maleville [23].

The choice of FD SOI combined to high $k$ and metal gate minimizes the need for channel doping, thus strongly reducing the dopant dependent $V_T$ variability and simplifying the metal gate processing. The reduction of $V_T$ scatter translates into a much more stable SRAM cell which is otherwise a serious issue beyond the 45 nm technology node for PD SOI and Si bulk based CMOS. Another significant advantage of a weakly doped channel is a much higher mobility, which in turn amplifies the stress induced mobility enhancement via local stressors or sSOI. Due to its SOI nature and improved gate control the FD device exhibits a very low leakage even at 125°C, thus also significantly lowering static power consumption by at least an order of magnitude compared to PD SOI or bulk CMOS.

Multi Gate FETs

The Multi Gate FET (MuGFET) or FinFETs are a vertical device approach that improves electrostatic control of a short transistor channel, while further increasing IC density. These devices are in the operation regime of 1V, and for fin thicknesses ranging from 10 to 40nm fully depleted devices. While the height of the fin is set by the Si thickness, the width control as well as the roughness of the fins becomes as critical as the thickness control for the planar FD devices. The manufacturability of MuGFETs is strongly dependent on the etch selectivity of the Si fins to the underlying buried oxide. Depending on the MuGFET design an undercut may be desired for gate underlap and
improved gate control. In order to add robustness to the fin formation with a highly reproducible underlap a thin buried silicon nitride can be added to the buried oxide in the fabrication of the starting SOI wafer. A further benefit of the composite dielectric nitride/oxide is to avoid the fin undercut during hydrogen sidewall smoothing of the fin’s sidewall lateral roughness [24]. Fins have been found to be very stable on the buried oxide much more than poly-silicon for equivalent film widths and thicknesses.

Figure 8. Schematic drawing of a FinFET with and without a composite dielectric nitride/oxide as an etch stop. The SEM micrograph shows an example of a composite nitride/oxide buried dielectric.

Advanced SOI Substrates

Capacitor less DRAMs

Circuit design has evolved to take advantage of the SOI properties and to optimize the area required per logic function. Capacitor-less one transistor DRAM cells are an important development which takes advantage of the floating body effect in SOI devices [25, 26]. The generation of excess negative or positive charge in the body can be used to store data states. In a n-channel device an excess of positive charges leads to an increase of the current drive, defining one state. The removal of positive charges from the body decreases the channel current, defining the opposite state. The industrial potential of the floating body cell (FBC) is important considering that it eliminates the process complexity associated to the stack or trench capacitor in a DRAM process. Very dense embedded memory blocks can be realized with standard SOI process with footprints as small as 4F², where F is the minimal feature size [25]. The development of the FBC technology is being attentively followed by the IC community. Recently a 128Mb FBC was reported [27] and its scalability to 32nm has been proven [28]. Further, the FBC concept has been proven to work as well for FinFET architecture [29]. The development of a capacitor less DRAM cell constitutes a breakthrough that can considerably reduce the cost of ownership of SOI technology with respect to its Si bulk equivalent and could enable a significant process simplification of today’s very complex DRAM ICs.

Ultra thin buried oxide SOI

Typical buried oxide (BOX) layer thicknesses for SOI are about 150nm or higher. The BOX reduction to 50nm or below enhances the parasitic device layer coupling with
the substrate, but for particular applications it may be the desired effect. For example for very low power applications, ultra-thin BOX offers the possibility to easily form buried n and p regions in the handle substrate, which can be used as back gates. By applying a back bias, the off current can be reduced by an order of magnitude or more, while in forward bias mode it lowers the device $V_T$, resulting in a current drive increase [30]. It is a particularly interesting concept for short channel effect control in a fully depleted MOSFET architecture and in low power SOC applications.

For ICs where local MOSFET self-heating can be a major concern, ultra thin BOX SOI may be an advantageous solution. A factor of 3 improvement in thermal conductance can be achieved by reducing the BOX thickness from 150nm to 20nm [31]. The tradeoff is, of course, increasing the parasitic junction capacitances.

For very low power SOCs, SOI with ultra thin buried oxide (<50nm) will enable IC architectures where n and p regions are defined in the handle substrate for back bias generation through the buried oxide. Since attaining the highest performance is not the focus here, these SOI CMOS solutions will target the lowest power consumption and longest battery lifetime. Low standby and low operating power devices will be built by taking full advantage of dielectric isolation.

**High Impedance SOI**

SOI offers design advantages over traditional bipolar devices resulting in a considerable reduction of crosstalk between RF analogue and digital logic elements plus easy integration with passive elements. High impedance SOI substrates enhance these advantages for mixed analogue/digital circuits combined to RF circuitry, voltage controlled oscillator (VCO) and low noise amplifiers (LNA), making them more robust to process variations [32].

High impedance SOI is an evolutionary SOI approach where the handle or base wafer is a high resistivity (HR) substrate (>1 kOhm-cm) [29]. SOI technology provides complete oxide isolation, cutting off direct paths of substrate injection noise and a high resistivity substrate reduces the capacitive coupling, further minimizing the substrate related RF loss. Because of the SOI nature of the high impedance substrate, latchup is of no concern, and ground shields can be avoided. Thus, higher density, smaller footprint mixed RF/analogue/digital IC can be achieved. Elimination of substrate crosstalk improves integrated passive components performance, becoming comparable to what can be achieved on InP [32].

CMOS SOI constitutes a cost effective alternative to GaAs and BiCMOS technologies [33]. Moreover, layer transfer offers the unique possibility to engineer SOI HR, high impedance substrates, to optimize RF gain, while reducing noise with no significant change in the fabrication process. SOI on high resistivity substrates (SOI-HR) [32] offers a solution tailored to RF applications that will substantially improve performance of passive components.
Conclusion

Engineered substrates offer disruptive, competitive advantages that enable heterogeneous integration and bridges towards new substrate functionality. In the field of microelectronics, substrate engineering is a proven path to reduce power consumption through enhanced mobility, dual surface orientation, fully depleted devices, high impedance substrates, etc. It opens new possibilities through added substrate functionality via buried dielectrics, band gap engineering, for improvement of the n- and p-channel devices adding robustness to the device fabrication. FD SOI or MuGFET architectures enables a further IC density while improving the device performance at the same time. The integration of embedded one transistor floating body memories on SOI will result in ICs that will not only have speed and power advantages, but should also be significantly lower cost.

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