Challenges and Opportunities for Electrochemical Processing in Microelectronics

Tom Ritzdorf
Semitool, 655 W. Reserve Dr., Kalispell, MT 59901
tritzdorf@semitool.com

Electrochemical deposition processes have become increasingly accepted in mainstream semiconductor and microelectronic processing over the last four decades. The most commonly discussed process is copper deposition for damascene interconnect manufacturing, but plating has also been used extensively for depositing metal layers in thin film recording heads, depositing solder alloys for flip chip bumps and for depositing gold conductors in III-V semiconductor devices. There are many other opportunities to utilize electrochemical processes in microelectronic manufacturing. This overview discusses some of the current development direction of processes currently in use, as well as some opportunities for implementing additional electrochemical processes in semiconductor processing.

Introduction

Electrochemical Deposition (ECD) has become a mainstream part of several microelectronic device manufacturing processes since its introduction about four decades ago. Through-mask electroplating was first used in the production of thin film recording heads in the late 1960’s and early 1970’s. Electrochemical deposition of gold has also been used for interconnects on III-V semiconductors, and electroplated solder alloys have been commonly used for flip chip applications. Copper ECD, in particular, has been studied extensively in its application to damascene interconnect processing. The science applied to this technology has greatly improved the mechanistic understanding of the copper ECD process over the last decade (1,2). While copper interconnect technology continues to advance and the reduction of feature sizes drives process improvements, this is far from the only place where electrochemical processing is beneficial for semiconductor and related microelectronics processing. There are many opportunities for utilizing electrochemical processes in microelectronic processing, and the list continues to grow.

Electrochemical processes include electrolytic deposition (electroplating), electroless deposition, and other anodic (oxidation) and cathodic (reduction) processes. Recently there has been interest in utilizing some of these electrochemical processes to take advantage of their specific capabilities or to provide inexpensive alternatives to vacuum processes. The following discussion will relate some of the opportunities and challenges currently being faced in semiconductor processing.
Thin Film magnetic Recording Heads

In the late 1960’s and early 1970’s IBM introduced the use of thin film microelectronic device processing to manufacture inductive thin film recording heads for hard disk drives. This “batch” manufacturing approach to building many heads in parallel on a single substrate was adopted by the industry by 1980, and through-mask electroplating of permalloy (80% nickel, 20% iron), copper and gold was used extensively in manufacturing these devices (3,4). This was the first large scale adoption of electrolytic processes for microelectronic manufacturing on substrates smaller than circuit boards. This led to the improvement of process control techniques and technical understanding of electrodeposition of metals and alloys, which would be necessary for more extensive adoption of electrochemical deposition (ECD) processes.

Figure 1. Thin film recording head for hard disk drive  (From Ref. 4, p. 318)

Gold Interconnects on Compound Semiconductors

The second high volume application of through-mask electrochemical deposition in microelectronics was for gold as conductors on gallium arsenide semiconductor devices. Again, photoresist masks on conductive seed layers were used to define the patterns for the metal deposition process (5). Gold conductors on the order of one micrometer in width and a similar deposition thickness have been used for GaAs based chips for over two decades. These conductors have typically been deposited using cyanide complexed
gold plating baths or gold sulfite based electrolytes. Superconformal deposition in recessed features has also been demonstrated using both of these chemistries (6,7).

![Figure 2. Through-mask plated gold conductor](image)

In addition to electrolytic deposition of gold for these conductors, it has been fairly common in the gold interconnect processing sequence on GaAs wafers to utilize an electrochemical process for the removal of the gold seed layer following the deposition of gold interconnects and the removal of the photoresist mask. This process typically utilized a thiourea and acid electrolyte to oxidize the gold seed layer (and a portion of the gold conductor) by making the wafer anodic to the counter-electrode. This process provides for additional control over chemical etching processes, as well as enabling the use of the electrical characteristics of the process for end point detection (See figure 3.).

![Figure 3. Chronopotentiometric traces of gold electrochemical etching processes for removal of gold seed layers.](image)
Chip Packaging Applications

ECD processes have been utilized in packaging applications for many years. The most common electrochemical process has been the electrolytic deposition of lead-tin solder alloys, however electroless deposition of nickel and gold or nickel, palladium, and gold has also been used for bonding or solder ball under bump metallurgy (UBM). There has been recent resurgence in some of these metallization schemes for bonding on top of copper metallization. There has also recently been much activity on the electrochemical deposition of lead-free solder alloys (8,9).

Electrolytic deposition of solder alloys has been used for many years for depositing eutectic and high-lead solder alloys for flip chip bonding of semiconductor devices (10). These alloys are commonly deposited from methane sulfonic acid based baths. The deposition process usually takes place within a thick photoresist template, with the thickness of the deposit sometimes exceeding the resist height to create a “mushroom” shape, as shown in figure 4. Recently, more focus has been given to lead-free solder alloys, such as tin-silver, with the focus of providing reliable processes with high deposition rates.

Figure 4. Cross-section of an electrochemically deposited solder bump with a thick copper plated stud.

Damascene Copper Interconnects

Copper interconnects for silicon based semiconductor devices were announced in 1997, and have been extensively adopted for logic chip manufacturing in the last decade. Copper interconnects continue to be driven to smaller feature sizes and new applications, which drives improvements in chemistry, processes, and process equipment. Memory-related applications like DRAM and flash memory currently drive the need for filling smaller features and handling increasing terminal effects. The potential difference between the center of the wafer and the cathode contacts at the edge of the wafer increases as the seed layer thickness decreases, and also as the pattern density increases. Features etched into the dielectric surface increase the resistance drop in two ways: by increasing the total distance the electrons must flow through the seed layer, and also by reducing the thickness of the conductive layer on the sidewalls of the features due to non-ideal step coverage. These effects drive equipment design to more adaptively control the
potential and current distributions across the wafer in order to be able to compensate for the terminal effect as it changes through the deposition process. Most equipment now has the capability to provide current distribution control through the use of multiple anodes and/or auxiliary cathodes, which act as current thieves. An additional advantage of using these systems is the ability to tailor the copper surface profile to complement the CMP process, which results in less dishing and erosion, and a tighter electrical distribution of the finished parts (11,12).

The effective resistivity of small lines is another issue that captures significant engineering attention these days. It is generally accepted that the circuit design will need to account for these effects as the linewidths approach the mean free path of an electron in copper. The challenge remains to reduce the effective resistivity of damascene lines, though, by decreasing the cross-sectional area of the barrier material in the lines and by improving the conductivity of the copper. One approach, as the line widths become very small, is to use alloying elements to adjust the mean free electron path and push back the point at which the resistivity starts increasing dramatically, as shown in figure 5. Although the bulk resistivity increases when alloying elements are added, the resistivity of a very thin film may actually be reduced. Other efforts to reduce resistivity focus on increasing the grain size, reducing incorporated contaminants and optimization of anneal steps.

Copper metallization processes are also being considered for contact vias to replace traditional tungsten plug vias in order to decrease contact resistance and alleviate fill limitations for very small vias. This is true for both memory and logic products. The challenges associated with using copper in the contact vias are that the barrier around and beneath the copper via must be very reliable, and the aspect ratio of these vias is higher than what is typically used in damascene interconnect processing, requiring a robust filling process. It has been shown that using copper in the contact module could potentially delay the resistance increases due to shrinking contacts by the equivalent of one technology node, or reduce contact resistance by about 40% (13,14).

Copper seed layer repair and direct on barrier (seedless) deposition processes provide opportunities to replace or augment vacuum deposition processes with electrochemical processes. These processes are being studied extensively, but have not yet been

Figure 5. Resistivity as a function of film thickness for copper and alloys containing 1% of the minor constituent.

Copper Alloy Resistivity as a Function of Film Thickness

![Copper Alloy Resistivity as a Function of Film Thickness](image-url)
incorporated into manufacturing due to the extension of PVD barrier and seed processes. Seed layer repair processes can be utilized to supplement PVD copper processes with conformally deposited copper to make the combined seed layer sufficient for copper fill processes(15).

Several groups have also been working on electrolytic or electroless copper deposition directly to barrier materials, including tantalum and ruthenium. These processes provide a potential route to overcome the sidewall coverage problems seen with PVD seed layer processes for very small features. Sidewall coverage of 75-90% have been achieved with electrolytic copper seed layer deposition directly on barriers, compared to the typical 10-20% step coverage seen in PVD processes(16). We have reported the ability to deposit copper directly to tantalum with adhesion of greater than 60 J/m² and excellent conformality (figure 6). These processes may soon be useful in production of semiconductor devices (17,18).

![Figure 6. Copper seed layer deposited directly to a tantalum barrier.](image)

**Contact Materials**

Salicide processes may provide another opportunity for selective electroless deposition. By depositing a controlled amount of Co, Ni, or Pt alloy selectively on the source, drain and polysilicon gate areas, this material can be used to create a silicide for the contact (19). Of course, the selectivity of the metal deposition must be excellent for this process to work well, and it is very difficult to develop a process that deposits equally on areas of the wafer regardless of doping. This differential doping effectively creates an electrical bias that must be overcome by the reducing agent(s) in the solution to cause deposition. There are also concerns related to depositing phosphorous or boron-doped alloys immediately above the doped silicon. If these materials diffuse into the silicon they will change the doping profiles of the source and drain regions and negatively impact transistor performance and yield.

**Platinum group metals**

Platinum group metals have also been used in various microelectronic applications, due to their corrosion resistance, solderability, and electrical characteristics. Platinum and ruthenium have been investigated for capacitor electrodes in memory storage capacitors utilizing high k dielectrics. ECD platinum has been investigated for this application (20). Palladium and rhodium have been considered or used for packaging and bonding applications for semiconductor chips. Other than the electrolytic or electroless deposition of Palladium for bonding or diffusion barrier in a bondable structure, however,
ECD processes for depositing the platinum group metals have not yet been extensively employed.

**Selective Barrier Capping**

Selective barrier deposition on copper interconnects is probably the second most studied ECD process in standard semiconductor processing. These selective barriers have been shown to result in dramatic increases in electromigration performance. They also hold the promise of decreasing the required thickness of dielectric barriers to provide a lower k-eff and RC product of the BEOL interconnect structure.

Typically these processes either use Pd-activated CoWP or self-activated CoWB alloys as the barrier to cap damascene copper lines. The palladium activated CoWP processes, as described by O’Sullivan, et al.(21), were utilized first, but they suffered from etching of the copper lines, which causes resistance increase, as well as an increase in leakage current due to deposition of metallic species on the dielectric surface. The resistance increase is due to the removal of copper during the palladium activation process, which replaces copper atoms with the more noble palladium. This is essentially an immersion deposition process, where the electrons necessary to reduce the palladium ions are contributed by the copper as it is oxidized and removed from the surface. The biggest problem seen with the removal of copper is usually micro-trenching of the copper near the barrier at the edges of lines.

Self-activated electroless barrier processes have been developed to overcome the problems mentioned above (fig. 7). These processes do not require the use of palladium nuclei for activation due to the use of a stronger reducing agent, typically dimethylamine borane (DMAB) or morpholine borane. These reducing agents will reduce the cobalt from solution to cause deposition even with copper as a catalytic surface. Hypophosphite is sometimes included to modify the alloy composition or to maintain the reaction rate without requiring large amounts of the more reactive boron-containing reducing agents.

![Figure 7. Cross-sectional TEM micrograph of self-activated cobalt alloy (259Å) deposited on copper.](image)

While there has been much activity on these selective capping processes, they have not been utilized in production environments, other than for CMOS image sensor applications (22). Modifications to the dielectric cap materials have helped to negate the
need for selective capping processes, which usually necessitate additional process steps and materials.

**Magnetic Materials**

Recently magnetic materials have been gaining interest in semiconductor manufacturing for several different applications. The most common application of magnetic alloys is in the manufacture of MRAM devices: as flux guides for the word line and bit line, or as shielding for the chip to eliminate interference from stray magnetic fields. Another application for magnetic alloys that is gaining interest is the fabrication of cores for high-Q inductors, which require high moment, resistive magnetic alloys (23). Depending on the application, these magnetic materials may be deposited electrolytically or electrolessly, and with or without an aligning magnetic field. Flux guides for MRAM drive lines have been deposited using electroless deposition, and shield material has been deposited electrolytically to thickness’ on the order of 20 µm.

**3D Interconnects**

3D interconnect processes have been receiving significant attention, both as a way to integrate multiple layers of active devices on a chip, and as a way to integrate multiple chips into stacked devices. Some of these integration schemes utilize electrodeposited copper to line or fill deep vias in the silicon to provide connection between active layers or chips (see figure 8). Although some of these structures look much like sub-micron damascene features, the processes required to fill them must be much different than the standard interconnect processes used for the last decade. The structures that are typically used for these applications are high aspect ratio vias that pass through the silicon. For chip-to-chip connections, these vias are usually between 50 µm and 250 µm deep, with aspect ratios between 5:1 and 15:1. Some are also considering structures with similar aspect ratios but with dimensions around one or two micrometers in diameter and 10 to 20 micrometers in depth, which could be used in various schemes to provide multiple active layers on a single chip.

![Figure 8](image_url)

*Figure 8. a. 60 µm x 250 µm via lined with copper, b. 10 µm x 100 µm via filled with copper.*
Electroformed Components

ECD processes have been used for electroforming in the microelectronics industry for several decades. Probably the most heavily-used electroforming process was the manufacture of stamping forms for the manufacture of compact disks. These nickel electroforming processes were used to produce compact disk masters, as well as to produce dependent parts that were used for stamping the plastic CDs. Micro-electroforming has also been used for producing various MEMS devices and has even been applied to novel structures for providing chip-to-package electrical connections. Recently, similar micro-electroforming processes have been utilized in the manufacture of probe tips for electrical test probe cards which are used for testing microelectronic devices, especially semiconductor chips.

![Electroformed probe card electrical contacts](image)

Figure 9. Electroformed probe card electrical contacts. (Courtesy of FormFactor)

Conclusions

ECD processes are becoming commonplace in microelectronics manufacturing. Furthermore, there are many opportunities to expand their use. The trend has reversed from trying to eliminate wet processing techniques to including them wherever they are advantageous in semiconductor processing. More electrochemical processes will probably be utilized in microelectronic manufacturing as time goes on.

Acknowledgments

The author would like to acknowledge contributions from the entire ECD Process organization at Semitool, who have made this work possible.
References


